HITACHI

SM012

42PD6700U

SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:
Before servicing this chassis, it is important that the service technician read the “Safety Precautions” and “Product Safety Notices” in this service manual.

ATTENTION:
Avant d’effectuer l’entretien du châassis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:
Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise“ und „Hinweise zur Produktsicherheit“ in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d’entretien peuvent faire l’objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

Plasma TV

June 2006

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2. SERVICE MENU ITEMS

2.1. SOUND 1

a) Menu Subwoofer => If ON, Subwoofer option is available in TV set, and the item is visible in sound menu, else Subwoofer is not available. Default “ON”.

b) Subwoofer Level (dB) => This value is gain value of Subwoofer output in dB. -30...12. Default “0” dB.

c) Subwoofer Corner Freq. (x10Hz) => Last low frequency value that is amplified. 5...40. Default “22” x 10Hz = 220Hz.

d) Menu Equalizer => If ON, visible in sound menu, else invisible. Default “ON”.

e) Menu Headphone => If ON, visible in sound menu, else invisible. Default “ON”.

f) Menu Effect => If ON, visible in sound menu, else invisible. Default “ON”.

g) Menu Wide Sound => If ON, visible in sound menu, else invisible. Default “OFF”.

h) Menu Dynamic Bass => If ON, visible in sound menu, else invisible. Default “ON”.

i) Menu Virtual Dolby => If ON, visible in sound menu, else invisible. Default “ON”.

j) Carrier Mute => If ON, in the absence of an FM carrier the output is muted, else not. Default “ON”.

k) Virtual Dolby Text => Active if VIRTUAL DOLBY is ON.According to the selection; seen in sound menu as 3DS or VIRTUAL DOLBY. Default “3DS”.

2.2. SOUND 2

a) AVL => AVL is controlled from this menu by service user. ON/OFF. Default “ON”.

b) Menu AVL => If ON, AVL item is visible in sound menu, and AVL can be controlled from sound menu by normal user, else AVL is invisible to normal user. ON/OFF. Default “ON”.

c) FM PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for the related standard. 0...127. Default “29”.

d) NICAM PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for the related standard. 0...127. Default “62”.

e) SCART PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for scart outputs. 0...127. Default “28”.

f) SCART VOLUME AVL ON => If AVL ON, set value in this item is used as volume value for scart1 and scart2. 0...127. Default “116”.

g) FM PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127. Default “15”.

h) NICAM PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127. Default “35”.

i) SCART PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for scart outputs. 0...127. Default “14”.

j) SCART VOLOUME AVL OFF => If AVL OFF, set value in this item is used as volume value for scart1 and scart2. 0...127. Default “122”.

2.3. Options

a) Burn-In Mode => If ON, full screen flashes in RED, GREEN, BLUE colors unless “Menu” button on Remote Control or Keypad is pressed. This property is used to protect the TV set from burning on the assembly lines in factory. This item becomes automatically OFF, when First APS item is ON or Factory Reset is pressed. ON/OFF. Default OFF.

b) First APS => This bit is set “ON” in the factory. When the TV set is opened for the first time it directs the user to make automatic search in both digital and analog modes.

c) APS Volume => After First APS function finishes, the volume of the TV is that value. Default “10”.

d) AGC (dB) => Tuner AGC value. Default “15”.

e) Power-Up Mode =>Normal, Last State, Stand-by. Default “Last State”

f) PDP Working Hour =>Displays Panel Run time in decimal.

g) Factory Reset => OK to activate. When OK pressed on this item, factory defaults loaded.

h) Enter Flash Mode =>OK to activate. When OK pressed on this item, flash mode is entered, SW starts to wait for uploading the new SW.

2.4. Features

a) Blue Background => If ON, Blue Background is visible in Features Menu else not. Default “ON”.

b) Menu Transparency => If ON, Menu Transparency is visible in Features Menu else not. Default “ON”.

c) Menu Timeout => If ON, Menu Timeout is visible in Features Menu else not. Default “ON”.

d) Backlight => If ON, Backlight is visible in Features Menu else not.Default “OFF”.

e) Single Tuner => If OFF, two tuners are available on the chassis. Fixed “ON”.

f) Dynamic WB => Default

2.5. Teletext

a) TOP TXT => ON/OFF

b) Fast TXT => ON/OFF

c) Teletext Language => Teletext Language may be controlled from this menu by service user.

d) Txt Start RF

e) Txt Start Ext

f) Txt Start Mix

g) Menu Teletext Language => If ON, Teletext Language item is visible in Features Menu, and Teletext Language can be controlled from Features Menu by normal user, else Teletext Language is invisible to normal user.

2.6. Tuner Options

a) Switch Low Band
b) Switch Mid Band
c) Switch High Band
d) Boundry1 Low Byte
e) Boundry1 High Byte
f) Boundry2 Low Byte
g) Boundry2 High Byte
h) Control Byte

These values need to be filled in the factory acording to the tuner used on the chassis.

i) Store => OK to store; when the values are entered correctly OK needs to be pressed on this item to store the values.

3. SOFTWARE UPDATE DESCRIPTION

3.1. ANALOG SOFTWARE UPDATE via SCART

STEP.1

Enter **service** menu by pressing the buttons ***"MENU","4","7","2","5"*** respectively.

STEP.2

Select **"OPTIONS"** from the service menu and **"ENTER FLASH MODE"**

STEP.3

Connect the Software Update Tool (17tr15-3) to parellel port of your PC.

STEP.4

Connect scart-end of the cable to Scart-1 (Ext-1).

STEP.5

Connect other-end of cable to **"PL 2"** socket on the Update Tool (17tr15-3)

STEP.6

Run **IAPWriter.exe.**

STEP.7

Click **"load file"** and load the required software.

3.2. ANALOG SOFTWARE UPDATE via I^2C

STEP.1

Enter service menu by pressing the buttons ***"MENU","4","7","2","5"*** respectively.

STEP.2

Select **"OPTIONS"** from the service menu and **"ENTER FLASH MODE"**

STEP.3

Connect the Software Update Tool (17tr15-3) to parellel port of your PC.

STEP.4

Connect one-end of cable to **"PL604"** socket on the chassis socket MB15

STEP.5

Connect other-end of cable to **"PL 2"** socket on the Update Tool (17tr15-3)

STEP.6

Run **IAPWriter.exe.**

STEP.7

Click **"load file"** and load the required software.

3.3. EEPROM UPDATE via SCART

STEP.1.

Insert the EEROM tool(TR16) to SCART-1

STEP.2.

Enter service menu by pressing the buttons ***"MENU","4","7","2","5"*** respectively

STEP.3.

Press **"YELLOW"** colour button on the remote controller.
Then you will have two options

STEP.3.a

Press **"RED"** colour button to copy data of external EEPROM into internal one

STEP.3.b

Press **"GREEN"** colour button to copy data of internal EEPROM into external one

4. INTRODUCTION

42" Plasma TV is a progressive TV control system with built-in **de-interlacer** and **scaler**. It uses a 1024x1024 panel with 16:9 aspect ratio.The TV is capable of operation in PAL, SECAM, NTSC (playback) colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Sound system output is supplying 2x10W (10%THD) for stereo 8Ω speakers. The chassis is equipped with many inputs and outputs allowing it to be used as a center of a media system.

It supports following peripherals:
2 SCART sockets
1 AV input (CVBS + Stereo Audio)
1 SVHS input
1 Stereo Headphone input
1 Component input (YPbPr + Stereo Audio)
1 D-Sub 15 PC input
1 HDMI input
1 Stereo audio input for PC
1 Stereo audio output
1 Subwoofer output

5. TUNER

The tuners used in the design are combined VHF, UHF tuners suitable for CCIR systems B/G, H, L, L', I/I', and D/K. The tuning is available through the digitally controlled I^2C bus (PLL). Below you will find info on one of the Tuners in use.

General description of UV1316:
The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

Features of UV1316:
1. Member of the UV1300 family small sized UHF/VHF tuners
2. Systems CCIR: B/G, H, L, L', I and I'; OIRT: D/K
3. Digitally controlled (PLL) tuning via I^2C-bus
4. Off-air channels, S-cable channels and Hyperband
5. World standardised mechanical dimensions and world standard pinning
6. Compact size
7. Complies to "CENELEC EN55020" and "EN55013"

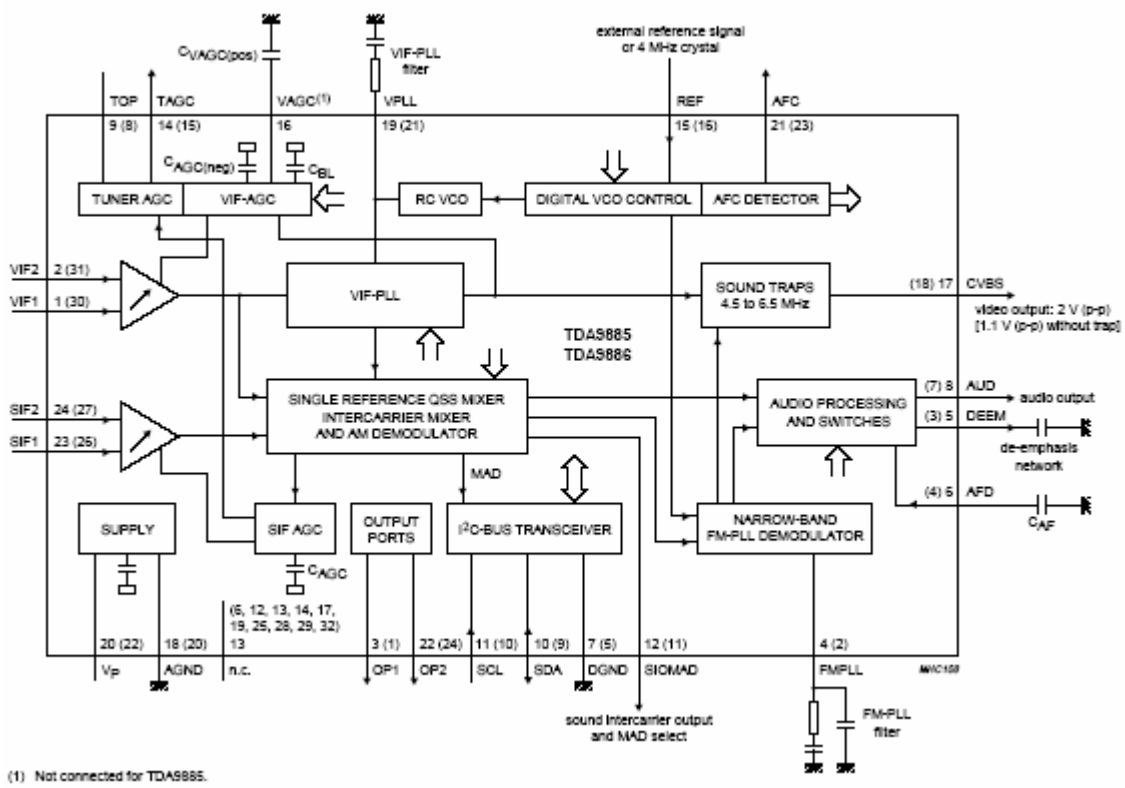
Pinning:

1.	Gain control voltage (AGC)	:	4.0V, Max: 4.5V
2.	Tuning voltage		
3.	I²C-bus address select	:	Max: 5.5V
4.	I²C-bus serial clock	:	Min:-0.3V, Max: 5.5V
5.	I²C-bus serial data	:	Min:-0.3V, Max: 5.5V
6.	Not connected		
7.	PLL supply voltage	:	5.0V, Min: 4.75V, Max: 5.5V
8.	ADC input		
9.	Tuner supply voltage	:	33V, Min: 30V, Max: 35V
10.	Symmetrical IF output 1		
11.	Symmetrical IF output 2		

6. IF PART (TDA9886)

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL. The following figure shows the simplified block diagram of the integrated circuit.
The integrated circuit comprises the following functional blocks:

VIF amplifier, Tuner and VIF-AGC, VIF-AGC detector, Frequency Phase-Locked Loop (FPLL) detector, VCO and divider, Digital acquisition help and AFC, Video demodulator and amplifier, Sound carrier trap, SIF amplifier, SIF-AGC detector, Single reference QSS mixer, AM demodulator, FM demodulator and acquisition help, Audio amplifier and mute time constant, I²C-bus transceivers and MAD (module address), Internal voltage stabilizer.



(1) Not connected for TDA9885.

7. MULTI STANDARD SOUND PROCESSOR

The MSP34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analogue TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analogue sound IF signal-in, down to processed analogue AF-out, is performed on a single chip.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free. Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x1G has optimum stereo performance without any adjustments.

8. VIDEO SWITCH TEA6415

In case of three or more external sources are used, the video switch IC TEA6415 is used. The main function of this device is to switch 8 video-input sources on the 6 outputs.

Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of sync. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB.For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external Resistor Bridge). All the switching possibilities are changed through the BUS. Driving 75ohm load needs an external resistor. It is possible to have the same input connected to several outputs.

9. AUDIO AMPLIFIER STAGE WITH TPA3004D2

The TPA3004D2 is a 12-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3004D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3004D2 eliminates the need for external heatsinks when playing music.

Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from –40 dB to 36 dB. Line outputs, for driving external headphone amplifier inputs, are also dc voltage controlled with a range of gain from –56 dB to 20 dB.

An integrated 5-V regulated supply is provided for powering an external headphone amplifier.

10. POWER SUPPLY (SMPS)

The DC voltages required at various parts of the chassis are provided by an SMPS transformer controlled by the IC MC44608, which is designed for driving, controlling and protecting switching transistor of SMPS. The transformer generates 145V for FBT input, +/-14V for audio amplifier, 5V and 3.3V stand by voltage and 8V, 12V and 5V supplies for other different parts of the chassis.

An optocoupler is used to control the regulation of line voltage and stand-by power consumption. There is a regulation circuit in secondary side. This circuit produces a control voltage according to the changes in 145V DC voltage, via an optocoupler (TCET1102G) to pin3 of the IC.

During the switch on period of the transistor, energy is stored in the transformer. During the switch off period energy is fed to the load via secondary winding. By varying switch-on time of the power transistor, it controls each portion of energy transferred to the second side such that the output voltage remains nearly independent of load variations.

11. MICROCONTROLLER

The Micronas SDA 55xx TV microcontroller is dedicated to 8 bit applications for TV control and provides dedicated graphic features designed for modern low class to mid range TV sets. The SDA 55xx provides also an integrated general purposefully 8051-compatible microcontroller with specific hardware features especially suitable in TV sets. The microcontroller core has been enhanced to provide powerful features such as memory banking, data pointers and additional interrupts, etc. The internal XRAM consists of up to 16 kBytes. The microcontroller provides an internal ROM of up to 128 kBytes. ROMless versions can access up to 1 MByte of external RAM and ROM. The 8-bit microcontroller runs at 33.33 MHz internal clock. SDA 55xx is realized in 0.25 micron technology with 2.5 V supply voltage for the core and 3.3 V for the I/O port pins to make them TTL compatible. Based on the SDA 55xx microcontroller the MINTS software package was developed and provides dedicated device drivers for many Micronas video & audio products and includes a full blown TV control SW for the PEPER application chassis. The SDA 55xx is also supported with powerful design tools like emulators from Hitex, Kleinhenz, iSystems, the Keil C51 Compiler and TEDIpro OSD development SW by Tara Systems.

12. SERIAL ACCESS CMOS 4Kx8(32KBit)EEPROM 24C32A

The Microchip Technology Inc. 24AA32A/24LC32A(24XX32A*) is a 32 Kbit Electrically Erasable PROM. The device is organized as four blocks of 8K x 8-bitmemory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1µA and 1mA, respectively. It has been developed for advanced, low-power applications such as personal communications or data acquisition. The 24XX32A also has a page write capability for up to 32 bytes of data. Functional address lines allow up to eight devices on the same bus, for up to 256Kbits address space.

13. CLASS AB STEREO HEADPHONE DRIVER TDA1308

The TDA1308 is an integrated class AB stereo headphone driver contained in a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

14. SAW FILTERS

K9656M:

Standard:

- B/G
- D/K
- I
- L/L'

Features

- TV IF audio filter with two channels
- Channel 1 (L') with one pass band for sound carriers at 40.40 MHz (L') and 39.75 MHz (L'- NICAM)
- Channel 2 (B/G, D/K, L, I) with one pass band for sound carriers between 32.35 MHz and 33.40 MHz

Terminals

- Tinned CuFe alloy

Pin configuration

1 Input
2 Switching input
3 Chip carrier - ground
4 Output
5 Output

K3958M:
Standard:
• B/G
• D/K
• I
• L/L'

Features
• TV IF video filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
• Constant group delay

Terminals
Tinned CuFe alloy

Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

15. IC DESCRIPTIONS

TEA6415C
24LC02
24C32
74LVC14A
TEA6420D
CS4334
GAL16LV8
K6R4008V1
KA278R33
LM1117
LM317T
LM809
MSP3411G
M29W040B
MC33202
PCF8574
TSOP1836
PI5V330
SDA5550
SII9993
SN74CB3Q3305
ST24LC21
LM2576
MC34063
TDA1308
TDA9886T
TPA3004D2
µPA672T
VPC3230D
MAD4868A
SVP EX-59B
TEA6415C

General Description
The main function of the IC is to switch 8 video input sources on 6 outputs. Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals). Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the alignment is switched off by forcing, with an external resistor bridge, 5 V_{DC} on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switching possibilities are changed through the BUS. Driving 75Ω load needs an external transistor. It is possible

to have the same input connected to several outputs. The starting configuration upon power on (power supply: 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configuration.

Features

- 20MHz Bandwidth
- Cascadable with another TEA6415C (Internal address can be changed by pin 7 voltage)
- 8 Inputs (CVBS, RGB, MAC, CHROMA,...)
- 6 Outputs
- Possibility of MAC or chroma signal for each input by switching-off the clamp with an external resistor bridge
- Bus controlled
- 6.5dB gain between any input and output
- 55dB crosstalk at 5mHz
- Fully ESD protected

Pinning

1.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max : 3mA
2.	Data	:	Low level	: -0.3V Max: 1.5V,
			High level	: 3.0V Max : Vcc+0.5V
3.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max : 3mA
4.	Clock	:	Low level	: -0.3V Max: 1.5V,
			High level	: 3.0V Max : Vcc+0.5V
5.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max : 3mA
6.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max : 3mA
7.	Prog			
8.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max: 3mA
9.	Vcc	:	12V	
10.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max : 3mA
11.	Input	:	Max	: 2Vpp, Input Current: 1mA, Max : 3mA
12.	Ground			
13.	Output	:	5.5Vpp,	Min : 4.5Vpp
14.	Output	:	5.5Vpp,	Min : 4.5Vpp
15.	Output	:	5.5Vpp,	Min : 4.5Vpp
16.	Output	:	5.5Vpp,	Min : 4.5Vpp
17.	Output	:	5.5Vpp,	Min : 4.5Vpp
18.	Output	:	5.5Vpp,	Min : 4.5Vpp
19.	Ground			
20.	Input	:	Max : 2Vpp, Input Current	: 1mA, Max : 3mA

15.1. 24LC02

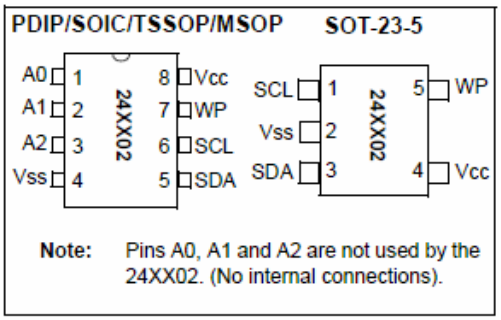
15.1.1. Description

The Microchip Technology Inc. 24AA02/24LC02B (24XX02*) is a 2 Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1µA and 1mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data.

15.1.2. Features

• Single supply with operation down to 1.8V
• Low-power CMOS technology
  -1mA active current typical
  -1µA standby current typical (I-temp)
• Organized as 1 block of 256 bytes (1 x 256 x 8)
• 2-wire serial interface bus, I^{2}C™ compatible
• Schmitt Trigger inputs for noise suppression
• Output slope control to eliminate ground bounce
• 100 kHz (24AA02) and 400 kHz (24LC02B) compatibility
• Self-timed write cycle (including auto-erase)
• Page write buffer for up to 8 bytes
• 2ms typical write cycle time for page write
• Hardware write-protect for entire memory
• Can be operated as a serial ROM
• Factory programming (QTP) available
• ESD protection > 4,000V
• 1,000,000 erase/write cycles
• Data retention > 200 years
• 8-lead PDIP, SOIC, TSSOP and MSOP packages
• 5-lead SOT-23 package
• Pb-free finish available
• Available for extended temperature ranges:
  -Industrial (I): -40°C to +85°C
  -Automotive (E): -40°C to +125°C

15.1.3. Pinning



Name	PDIP	SOIC	TSSOP	MSOP	SOT23	Description
A0	1	1	1	1	—	Not Connected
A1	2	2	2	2	—	Not Connected
A2	3	3	3	3	—	Not Connected
Vss	4	4	4	4	2	Ground
SDA	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	1	Serial Clock
WP	7	7	7	7	5	Write-Protect Input
Vcc	8	8	8	8	4	+1.8V to 5.5V Power Supply

15.2. 24C32

15.2.1. General Description

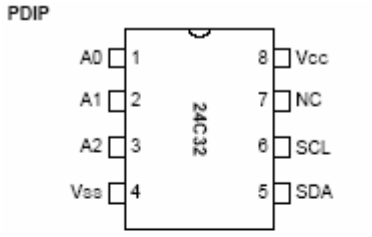
The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to 8 - 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications.

15.2.2. Features

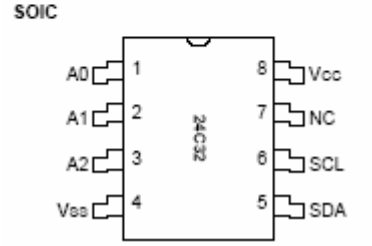
• Voltage operating range: 4.5V to 5.5V
  - Peak write current 3 mA at 5.5V
  - Maximum read current 150µA at 5.5V
  - Standby current 1µA typical
• Industry standard two-wire bus protocol, I^2C™ compatible
  -Including 100 kHz and 400 kHz modes
• Self-timed write cycle (including auto-erase)
• Power on/off data protection circuitry
• Endurance:
  - 10,000,000 Erase/Write cycles guaranteed for High Endurance Block
  - 10,000,000 E/W cycles guaranteed for Standard Endurance Block
• 8 byte page, or byte modes available
• 1 page x 8 line input cache (64 bytes) for fast write
loads
• Schmitt trigger, filtered inputs for noise suppression
• Output slope control to eliminate ground bounce
• 2 ms typical write cycle time, byte or page
• Up to 8 chips may be connected to the same bus for up to 256K bits total memory
• Electrostatic discharge protection > 4000V
• Data retention > 200 years
• Temperature ranges:
  -Commercial (C): 0°C to +70°C
  -Industrial (I): -40°C to +85°C

15.2.3. Pinning

PDIP



SOIC



15.2.4. PIN Function Table

Name	Function
A0..A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

PIN DESCRIPTIONS

A0, A1, A2 Chip Address Inputs

The A0...A2 inputs are used by the 24C32 for multiple device operation and conform to the two-wire bus standard. The levels applied to these pins define the address block occupied by the device in the address map. A particular device is selected by transmitting the corresponding bits (A2, A1, and A0) in the control byte.

SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal; therefore the SDA bus requires a pull-up resistor to VCC (typical 10KQ for 100 kHz, 1KQ for 400 kHz). For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

15.3. 74LVC14A

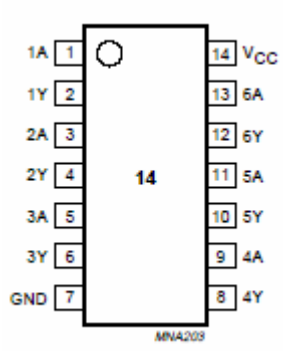
15.3.1. Description

The 74LVC14A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5V environment. The 74LVC14A provides six inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

15.3.2. Features

- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no.8-1A
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000V
  - MM EIA/JESD22-A115-A exceeds 200V.
- Specified from -40 to +85C and -40 to +125C.

15.3.3. Pinning



PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V_{CC}	supply voltage

15.4. TEA6420

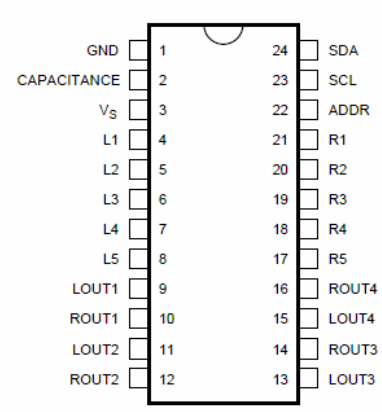
15.4.1. Features

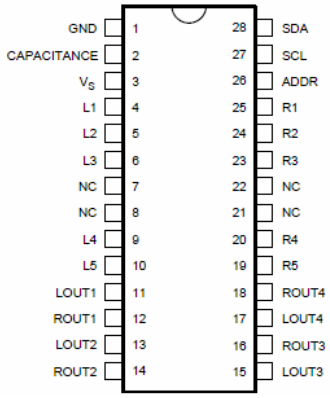
• 5 Stereo Inputs
• 4 Stereo Outputs
• Gain Control 0/2/4/6dB/Mute for each Output
• Cascadable (2 different addresses)
• Serial Bus Controlled
• Very low Noise
• Very low Distortion

15.4.2. Description

The TEA6420 switches 5 stereo audio inputs on4stereo outputs. All the switching possibilities are changed through the I^2C bus.

15.4.3. Pin Connections





15.5. CS4334

15.5.1. Features

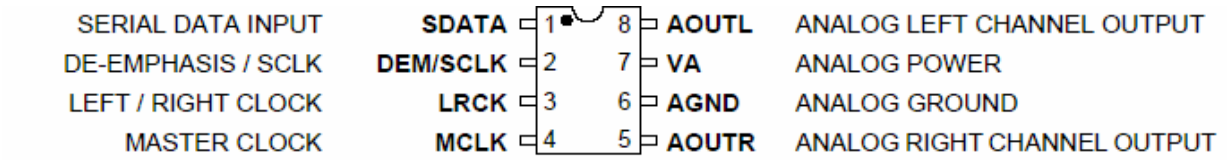
• Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
• 24-Bit Conversion

• 96 dB Dynamic Range
• -88 dB THD+N
• Low Clock Jitter Sensitivity
• Single +5V Power Supply
• Filtered Line Level Outputs
• On-Chip Digital De-emphasis
• Popgaurd® Technology
• Functionally Compatible with CS4330/31/33

15.5.2. General Description

The CS4334 family members are complete, stereo digital-to-analog output systems including interpolation, 1-bitD/A conversion and output analog filtering in an 8-pinpackage. The CS4334/5/6/7/8/9 support all major audio data interface formats, and the individual devices differ only in the supported interface format. The CS4334 family is based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency. The CS4334 family contains on-chip digital de-emphasis, operates from a single +5V power supply, and requires minimal support circuitry. These features are ideal for set-top boxes, DVD players, SVCD players, and A/V receivers.

15.5.3. Pin Descriptions



No.	Pin Name	I/O	Pin Function and Description
1	SDATA	I	***Serial Audio Data Input*** - two's complement MSB-first serial data is input on this pin. The data is clocked into the CS4334/5/6/7/8/9 via internal or external SCLK, and the channel is determined by LRCK.
2	DEM/SCLK	I	***De-Emphasis/External Serial Clock Input*** - used for de-emphasis filter control or external serial clock input.
3	LRCK	I	***Left/Right Clock*** - determines which channel is currently being input on the Audio Serial Data Input pin, SDATA.
4	MCLK	I	***Master Clock*** - frequency must be 256x, 384x, or 512x the input sample rate in BRM and either 128x or 192x the input sample rate in HRM.
5	AOUTR	O	***Analog Right Channel Output*** - typically 3.5 Vp-p for a full-scale input signal.
6	AGND	I	***Analog Ground*** - analog ground reference is 0V.
7	VA	I	***Analog Power*** - analog power supply is nominally +5V.
8	AOUTL	O	***Analog Left Channel Output*** - typically 3.5 Vp-p for a full-scale input signal.

15.6. GAL16LV8

15.6.1. Description

The GAL16LV8D, at 3.5 ns maximum propagation delay time, provides the highest speed performance available in the PLD market. The GAL16LV8C can interface with both 3.3V and 5Vsignal levels. The GAL16LV8 is manufactured using Lattice Semiconductor's advanced 3.3V E^2CMOS process, which combines CMOS with Electrically Erasable (E^2) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.
The 3.3V GAL16LV8 uses the same industry standard 16V8 architecture as its 5V counterpart and supports all architectural features such as combinatorial or registered macrocell operations.
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

15.6.2. Features

• HIGH PERFORMANCE E2CMOS® TECHNOLOGY
  - 3.5 ns Maximum Propagation Delay
  - Fmax = 250 MHz

- 2.5 ns Maximum from Clock Input to Data Output
- UltraMOS® Advanced CMOS Technology

• 3.3V LOW VOLTAGE 16V8 ARCHITECTURE
- JEDEC-Compatible 3.3V Interface Standard
- 5V Compatible Inputs
- I/O Interfaces with Standard 5V TTL Devices (GAL16LV8C)

• ACTIVE PULL-UPS ON ALL PINS (GAL16LV8D Only)

• E2 CELL TECHNOLOGY
- Reconfigurable Logic
- Reprogrammable Cells
- 100% Tested/100% Yields
- High Speed Electrical Erasure (<100ms)
- 20 Year Data Retention

• EIGHT OUTPUT LOGIC MACROCELLS
- Maximum Flexibility for Complex Logic Designs
- Programmable Output Polarity

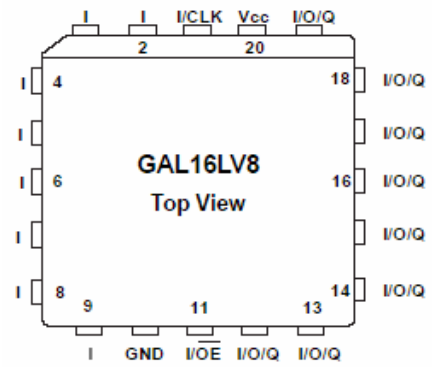
• PRELOAD AND POWER-ON RESET OF ALL REGISTERS
- 100% Functional Testability

• APPLICATIONS INCLUDE:
- Glue Logic for 3.3V Systems
- DMA Control
- State Machine Control
- High Speed Graphics Processing
- Standard Logic Speed Upgrade

• ELECTRONIC SIGNATURE FOR IDENTIFICATION

• LEAD-FREE PACKAGE OPTIONS

15.6.3. Pin connections



15.7.

15.8. K6R4008V1D

15.8.1. Description

The K6R4008V1D is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. TheK6R4008V1D uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG′s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4008V1D is packaged in a 400 mil 36-pin plastic SOJ and 44-pin plastic TSOP type II.

15.8.2. Features

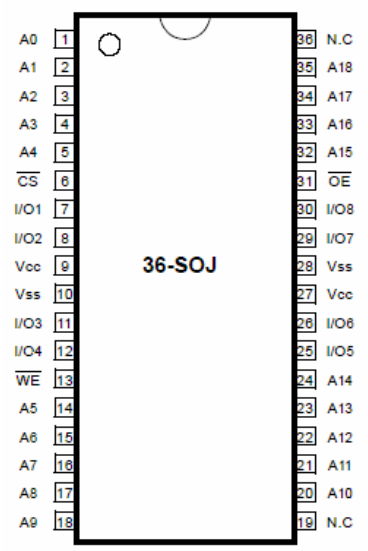
• Fast Access Time 8, 10ns(Max.)

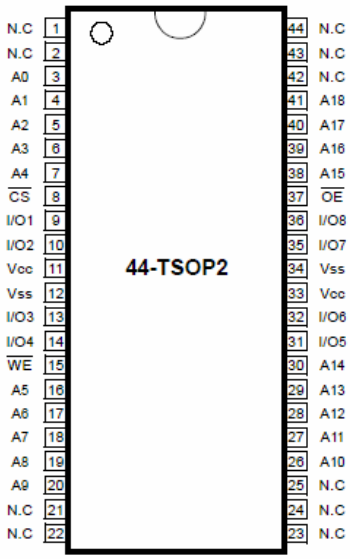
• Low Power Dissipation
- Standby (TTL) : 20mA(Max.)
(CMOS) : 5mA(Max.)
- Operating K6R4008V1D-08 : 80mA(Max.)

K6R4008V1D-10 : 65mA(Max.)

- Single 3.3 ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - K6R4008V1D-J : 36-SOJ-400
  - K6R4008V1D-K : 36-SOJ-400(Lead-Free)
  - K6R4008V1D-T : 44-TSOP2-400BF
  - K6R4008V1D-U : 44-TSOP2-400BF(Lead-Free)
- Operating in Commercial and Industrial Temperature range.

15.8.3. Pin Description





Pin Name	Pin Function
A_0 - A_{18}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1 ~ I/O_8	Data Inputs/Outputs
V_{CC}	Power(+3.3V)
V_{SS}	Ground
N.C	No Connection

15.9. KA278R33

15.9.1. Features

- 2A / 3.3V Output low dropout voltage regulator
- TO220 Full-Mold package (4PIN)
- Overcurrent protection, Thermal shutdown
- Overvoltage protection, Short-Circuit protection
- With output disable function

15.9.2. Description

The KA278R33 is a low-dropout voltage regulator suitable for various electronic equipments. It provides constant voltage power source with TO-220 4 lead full mold package. Dropout voltage of KA278R33 is below

0.5V in full rated current (2A). This regulator has various function such as peak current protection, thermal shut down, overvoltage protection and output disable function.

15.10. LM1117

15.10.1. General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.
The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to as-sure output voltage accuracy to within ±1%. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10μF tantalum capacitor is required at the output to improve the transient response and stability.

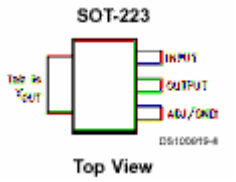
15.10.2. Features

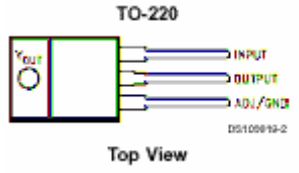
• Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
• Space Saving SOT-223 Package
• Current Limiting and Thermal Protection
• Output Current 800mA
• Line Regulation 0.2% (Max)
• Load Regulation 0.4% (Max)
• Temperature Range
— LM1117 0°C to 125°C
— LM1117I -40°C to 125°C

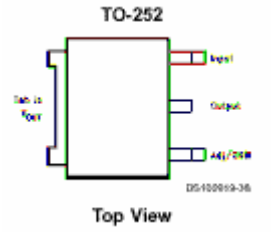
15.10.3. Applications

• 2.85V Model for SCSI-2 Active Termination
• Post Regulator for Switching DC/DC Converter
• High Efficiency Linear Regulators
• Battery Charger
• Battery Powered Instrumentation

Connection Diagrams







15.11. LM317

15.11.1. General Description

This monolithic integrated circuit is an adjustable 3-terminal positive voltage regulator designed to supply more than 1.5A of load current with an output voltage adjustable over a 1.2 to 37V. It employs internal current limiting, thermal shut-down and safe area compensation.

15.11.2. Features

• Output Current In Excess of 1.5A
• Output Adjustable Between 1.2V and 37V
• Internal Thermal Overload Protection
• Internal Short Circuit Current Limiting
• Output Transistor Safe Operating Area Compensation
• TO-220 Package

15.11.3. Pin Description

TO-220

1. Adj 2. Output 3. Input

15.12. LM809

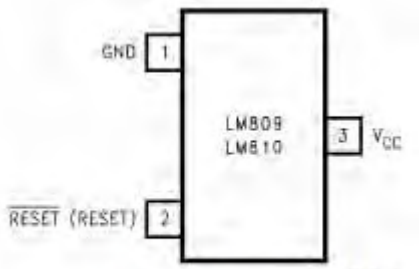
15.12.1. General Description

The LM809/810 microprocessor supervisory circuits can be used to monitor the power supplies in microprocessor and digital systems. They provide a reset to the microprocessor during power-up, power-down and brown-out conditions. The function of the LM809/810 is to monitor the VCC supply voltage, and assert a reset signal whenever this voltage declines below the factory-programmed reset threshold. The reset signal remains asserted for 240 ms after VCC rises above the threshold. The LM809 has an active-low RESET output, while the LM810 has an active-high RESET output. Seven standard reset voltage options are available, suitable for monitoring 5V, 3.3V, and 3V supply voltages. With a low supply current of only 15µA, the LM809/810 are ideal for use in portable equipment.

15.12.2. Features

- Precise monitoring of 3V, 3.3V, and 5V supply voltages
- Superior upgrade to MAX809/810
- Fully specified overtemperature
- 140 ms min. Power-On Reset pulse width, 240 ms typical
  - Active-low RESET Output(LM809)
  - Active-high RESET Output(LM810)
- Guaranteed RESET Output valid for VCC≥1V
- Low Supply Current, 15µAtyp
- Power supply transient immunity

15.12.3. Pinning



( ) are for LM810

PIN		NAME	FUNCTION
(LLP)	SOT-23		
1	1	GND	Ground reference
3	2	$\overline{RESET}$ (LM809)	Active-low output. $\overline{RESET}$ remains low while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
		RESET (LM810)	Active-high output. RESET remains high while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
5	3	V_{CC}	Supply Voltage (+5V, +3.3V, or +3.0V)

15.13. MSP34X1G (MSP3411G)

Multistandard Sound Processor Family

15.13.1. Introduction

The MSP 34x1G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure shows a simplified functional block diagram of the MSP 34x1G.

The MSP 34x1G has all functions of the MSP 34x0G with the addition of a virtual surround sound feature.

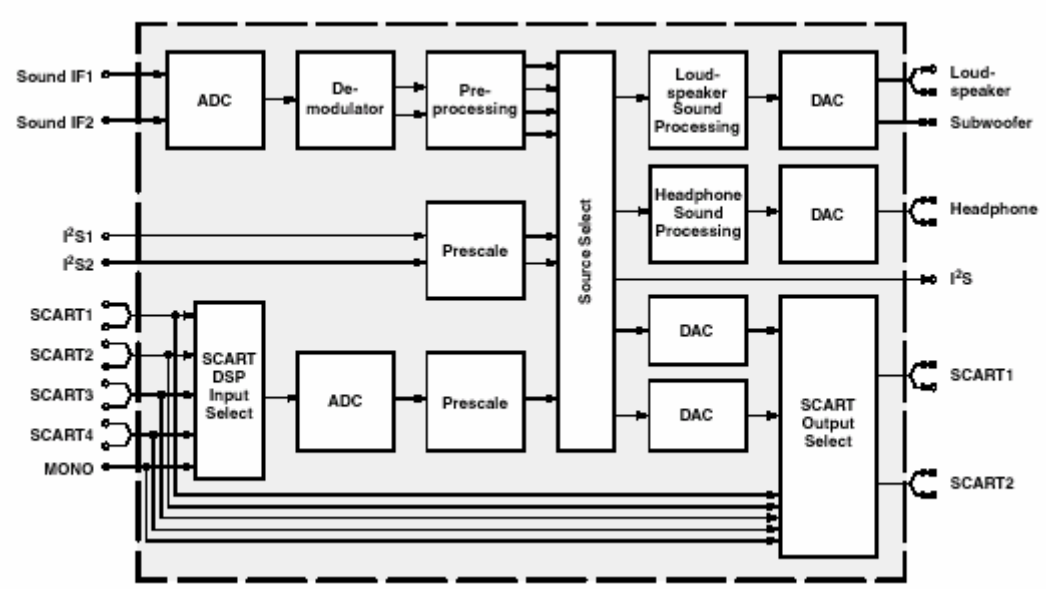
Surround sound can be reproduced to a certain extent with two loudspeakers. The MSP 34x1G includes the Micronas virtualizer algorithm “3D-PANORAMA” which has been approved by the Dolby 1) Laboratories for with the "Virtual Dolby Surround" technology. In addition, the MSP 34x1G includes the “PAN-ORAMA” algorithm.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x1G has optimum stereo performance without any adjustments.

The MSP 34x1G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I 2 C interaction is necessary (Automatic Sound Selection).



Source Select

I^2S bus interface consists of five pins:

1. I2S_DA_IN1, I2S_DA_IN2: For input, four channels (two channels per line, 2*16 bits) per sampling cycle (32 kHz) are transmitted.
2. I2S_DA_OUT: For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.
3. I2S_CL: Gives the timing for the transmission of I^2S serial data (1.024 MHz).
4. I2S_WS: The I2S_WS word strobe line defines the left and right sample.

15.13.2. Features

- Standard Selection with single I^2C transmission
- Automatic Standard Detection of terrestrial TV standards
- Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS
- Two selectable sound IF (SIF) inputs
- Automatic Carrier Mute function
- Interrupt output programmable (indicating status change)
- Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness
- AVC: Automatic Volume Correction
- Subwoofer output with programmable low-pass and complementary high-pass filter
- 5-band graphic equalizer for loudspeaker channel
- Spatial effect for loudspeaker channel
- Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs

• Complete SCART in/out switching matrix
• Two I^2S inputs; one I^2S output
• Dolby Pro Logic with DPL 351xA coprocessor
• All analog FM-Stereo A2 and satellite standards; AM-SECAM L standard
• Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM
• Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification)
• ASTRA Digital Radio (ADR) together with DRP 3510A
• All NICAM standards
• Korean FM-Stereo A2 standard

Pin connections

NC = not connected; leave vacant

LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin	PLQFP 64-pin				
1	16	14	9	8	ADR_WS	OUT	LV	ADR word strobe
2	-	-	-	-	NC		LV	Not connected
3	15	13	8	7	ADR_DA	OUT	LV	ADR Data Output
4	14	12	7	6	I2S_DA_IN1	IN	LV	I^2S1 data input
5	13	11	6	5	I2S_DA_OUT	OUT	LV	I^2S data output
6	12	10	5	4	I2S_WS	IN/OUT	LV	I^2S word strobe
7	11	9	4	3	I2S_CL	IN/OUT	LV	I^2S clock
8	10	8	3	2	I2C_DA	IN/OUT	OBL	I^2C data
9	9	7	2	1	I2C_CL	IN/OUT	OBL	I^2C clock
10	8	-	1	64	NC		LV	Not connected
11	7	6	80	63	STANDBYQ	IN	OBL	Stand-by (low-active)
12	6	5	79	62	ADR_SEL	IN	OBL	I^2C bus address select
13	5	4	78	61	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
14	4	3	77	60	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
15	3	-	76	59	NC		LV	Not connected
16	2	-	75	58	NC		LV	Not connected
17	-	-	-	-	NC		LV	Not connected
18	1	2	74	57	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
19	64	1	73	56	TP		LV	Test pin
20	63	52	72	55	XTAL_OUT	OUT	OBL	Crystal oscillator
21	62	51	71	54	XTAL_IN	IN	OBL	Crystal oscillator
22	61	50	70	53	TESTEN	IN	OBL	Test pin
23	60	49	69	52	ANA_IN2+	IN	AVSS via 56 pF/LV	IF Input 2 (can be left vacant, only if IF input 1 is also not in use)
24	59	48	68	51	ANA_IN-	IN	AVSS via 56 pF/LV	IF common (can be left vacant, only if IF input 1 is also not in use)
25	58	47	67	50	ANA_IN1+	IN	LV	IF input 1
26	57	46	66	49	AVSUP		OBL	Analog power supply 5V
-	-	-	65	-	AVSUP		OBL	Analog power supply 5V
-	-	-	64	-	NC		LV	Not connected
-	-	-	63	-	NC		LV	Not connected
27	56	45	62	48	AVSS		OBL	Analog ground
-	-	-	61	-	AVSS		OBL	Analog ground
28	55	44	60	47	MONO_IN	IN	LV	Mono input
-	-	-	59	-	NC		LV	Not connected
29	54	43	58	46	VREFTOP		OBL	Reference voltage IF A/D converter
30	53	42	57	45	SC1_IN_R	IN	LV	SCART 1 input, right
31	52	41	56	44	SC1_IN_L	IN	LV	SCART 1 input, left
32	51	-	55	43	ASG1		AHVSS	Analog Shield Ground 1
33	50	40	54	42	SC2_IN_R	IN	LV	SCART 2 input, right
34	49	39	53	41	SC2_IN_L	IN	LV	SCART 2 input, left
35	48	-	52	40	ASG2		AHVSS	Analog Shield Ground 2
36	47	38	51	39	SC3_IN_R	IN	LV	SCART 3 input, right

37	46	37	50	38	SC3_IN_L	IN	LV	SCART 3 input, left
38	45	-	49	37	ASG4		AHVSS	Analog Shield Ground 4
39	44	-	48	36	SC4_IN_R	IN	LV	SCART 4 input, right
40	43	-	47	35	SC4_IN_L	IN	LV	SCART 4 input, left
41	-	-	46	-	NC		LV or AHVSS	Not connected
42	42	36	45	34	AGNDC		OBL	Analog reference voltage
43	41	35	44	33	AHVSS		OBL	Analog ground
-	-	-	43	-	AHVSS		OBL	Analog ground
-	-	-	42	-	NC		LV	Not connected
-	-	-	41	-	NC		LV	Not connected
44	40	34	40	32	CAPL_M		OBL	Volume capacitor MAIN
45	39	33	39	31	AHVSUP		OBL	Analog power supply 8V
46	38	32	38	30	CAPL_A		OBL	Volume capacitor AUX
47	37	31	37	29	SC1_OUT_L	OUT	LV	SCART output 1, left
48	36	30	36	28	SC1_OUT_R	OUT	LV	SCART output 1, right
49	35	29	35	27	VREF1		OBL	Reference ground 1
50	34	28	34	26	SC2_OUT_L	OUT	LV	SCART output 2, left
51	33	27	33	25	SC2_OUT_R	OUT	LV	SCART output 2, right
52	-	-	32	-	NC		LV	Not connected
53	32	-	31	24	NC		LV	Not connected
54	31	26	30	23	DACM_SUB	OUT	LV	Subwoofer output
55	30	-	29	22	NC		LV	Not connected
56	29	25	28	21	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	20	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	19	VREF2		OBL	Reference ground 2
59	26	22	25	18	DACA_L	OUT	LV	Headphone out, left
60	25	21	24	17	DACA_R	OUT	LV	Headphone out, right
-	-	-	23	-	NC		LV	Not connected
-	-	-	22	-	NC		LV	Not connected
61	24	20	21	16	RESETQ	IN	OBL	Power-on-reset
62	23	-	20	15	NC		LV	Not connected
63	22	-	19	14	NC		LV	Not connected
64	21	19	18	13	NC		LV	Not connected
65	20	18	17	12	I2S_DA_IN2	IN	LV	I^2S2-data input
66	19	17	16	11	DVSS		OBL	Digital ground
-	-	-	15	-	DVSS		OBL	Digital ground
-	-	-	14	-	DVSS		OBL	Digital ground
67	18	16	13	10	DVSUP		OBL	Digital power supply 5V
-	-	-	12	-	DVSUP		OBL	Digital power supply 5V
-	-	-	11	-	DVSUP		OBL	Digital power supply 5V
68	17	15	10	9	ADR_CL	OUT	LV	ADR clock

15.14. M29W040B

15.14.1. Description

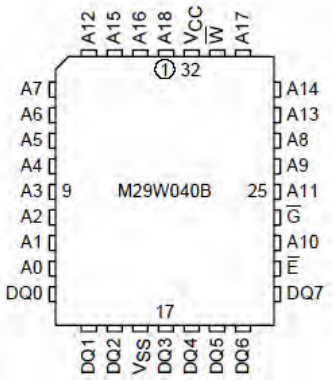
The M29W040B is a 4 Mbit (512Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM. The M29W040B is fully backward compatible with the M29W040.The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are writ-ten to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards. Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

15.14.2. Features

• SINGLE 2.7 to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
• ACCESS TIME: 55ns
• PROGRAMMING TIME
  - 10µs per Byte typical8
• UNIFORM 64 Kbytes MEMORY BLOCKS
• PROGRAM/ERASE CONTROLLER
  - Embedded Byte Program algorithm
  - Embedded Multi-Block/Chip Erase algorithm
  - Status Register Polling and Toggle Bits

• ERASE SUSPEND and RESUME MODES
    - Read and Program another Block during Erase Suspend
• UNLOCK BYPASS PROGRAM COMMAND
    - Faster Production/Batch Programming
• LOW POWER CONSUMPTION
    - Standby and Automatic Standby
• 100,000 PROGRAM/ERASE CYCLES per BLOCK
• 20 YEARS DATA RETENTION
    - Defectivity below 1 ppm/year
• ELECTRONIC SIGNATURE
    - Manufacturer Code: 20h
    - Device Code: E3h

15.14.3. Pin Descriptions



A0-A18	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

15.15. MC33202

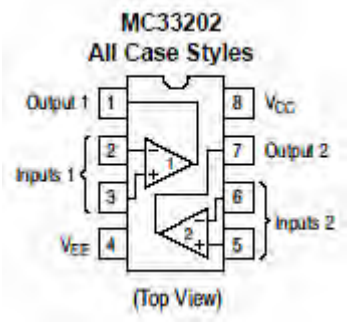
15.15.1. General Description

The MC33201/2/4 family of operational amplifiers provide rail−to−rail operation on both the input and output. The inputs can be driven as high as 200mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail−to−rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (±0.9 V) yet can operate with a supply of up to +12V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

15.15.2. Features

• Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
• Input Voltage Range Includes both Supply Rails
• Output Voltage Swings within 50 mV of both Rails
• No Phase Reversal on the Output for Over−driven Input Signals
• High Output Current (ISC = 80 mA, Typ)
• Low Supply Current (ID = 0.9 mA, Typ)
• 600 Ω Output Drive Capability
• Extended Operating Temperature Ranges (−40° to +105°C and −55° to +125°C)
• Typical Gain Bandwidth Product = 2.2 MHz
• Pb−Free Packages are Available

15.15.3. Pin Connections



15.16. PCF8574

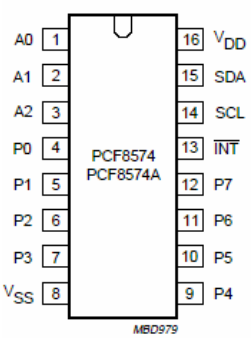
15.16.1. General Description

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I^2C).The device consists of an 8-bit quasi-bidirectional port and an I^2C-bus interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the PCF8574 can remain a simple slave device.

15.16.2. Features

- Operating supply voltage 2.5 to 6V
- Low standby current consumption of 10 μA maximum
- I^2C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O port for the I^2C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, or space-saving SO16 or SSOP20 packages.

15.16.3. Pinning



SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O 0
P1	5	11	quasi-bidirectional I/O 1
P2	6	12	quasi-bidirectional I/O 2
P3	7	14	quasi-bidirectional I/O 3
V_{SS}	8	15	supply ground
P4	9	16	quasi-bidirectional I/O 4
P5	10	17	quasi-bidirectional I/O 5
P6	11	19	quasi-bidirectional I/O 6
P7	12	20	quasi-bidirectional I/O 7
$\overline{INT}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V_{DD}	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected

15.17. TSOP1836

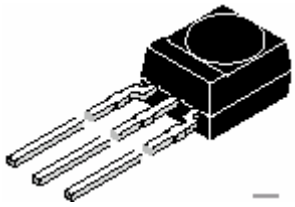
15.17.1. Description

The TSOP18.– series are miniaturized receivers for infrared remote control systems. PIN diode and preamplifier are assembled on lead frame, the epoxy package is designed as IR filter. Carrier frequency for TSOP1836 is 36 kHz.

The demodulated output signal can directly be decoded by a microprocessor. The main benefit is the reliable function even in disturbed ambient and the protection against uncontrolled output pulses.

15.17.2. Features

• Photo detector and preamplifier in one package
• Internal filter for PCM frequency
• TTL and CMOS compatibility
• Output active low
• Improved shielding against electrical field disturbance
• Suitable burst length .6 cycles/burst



Special Features

• Small size package
• Enhanced immunity against all kinds of disturbance light
• No occurrence of disturbance pulses at the output
• Short settling time after power on (<200_s)

15.18. PI5V330

15.18.1. General Description

The PI5V330 is well suited for video applications when switching composite or RGB analogue. A picture-in-picture application will be described in this brief. The pixel-rate creates video overlays so two or more pictures can be viewed at the same time. An inexpensive NTSC titler can be implemented by superimposing the output of a character generator on a standard composite video background.

15.19. SDA55XX (SDA5550)

15.19.1. General description

The SDA55XX is a single chip teletext decoder for decoding World System Teletext data as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide Screen Signalling (WSS) data used for PAL plus transmissions (Line 23). The device also supports Closed caption acquisition and decoding. The device provides an integrated general-purpose, fully 8051-compatible Microcontroller with television specific hardware features. Microcontroller has been enhanced to provide powerful features such as memory banking, data pointers, and additional interrupts etc. The on-chip display unit for displaying Level 1.5 teletext data can also be used for customer defined on screen displays. Internal XRAM consists of up to16 Kbytes. Device has an internal ROM of up to 128 KBytes. ROMless versions can access up to 1 MByte of external RAM and ROM. The SDA 55XX supports a wide range of standards including PAL, NTSC and contains a digital slicer for VPS, WSS, PDC, TTX and Closed Caption, an accelerating acquisition hardware module, a display generator for Level 1.5 TTX data and powerful On screen Display capabilities based on parallel attributes, and Pixel oriented characters (DRCS).
The 8-bit Microcontroller runs at 360 ns. cycle time (min.). Controller with dedicated hardware does most of the internal TTX acquisition processing, transfers data to/from external memory interface and receives/ transmits data via I^2C-firmware user-interface. The slicer combined with dedicated hardware stores TTX data in a VBI buffer of 1 Kilobyte. The Microcontroller firmware performs all the acquisition tasks (hamming and parity-checks, page search and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26-handling, FLOF, TOP and list-pages. The interface to user software is optimized for minimal overhead. SDA 55XX is realized in 0.25 micron technology with 2.5 V supply voltage and 3.3 V I/O (TTL compatible). The software and hardware development environment (TEAM) is available to simplify and speed up the development of the software and On Screen Display. TEAM stands for TVT Expert Application Maker. It improves the TV controller software quality in following aspects:
– Shorter time to market
– Re-usability
– Target independent development
– Verification and validation before targeting
– General test concept
– Graphical interface design requiring minimum programming and controller know how.
– Modular and open tool chain, configurable by customer.

15.20. SiI 9993

15.20.1. General Description

The SiI 9993 is the first generation of PanelLink receivers that are designed for the HDMI 1.0 (High Definition Multimedia Interface) specification. DTVs, plasma displays, LCD TVs and projectors can now provide the purest level of protected digital audio/video over a simple, low cost cable. Backwards compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 host (DVD players, HD set top boxes, D-VHS players and receivers, PC). The SiI 9993 incorporates a flexible audio and video interface. The receiver can connect to RGB input and output YCbCr using an integrated color space converter. This allows full backward compatibility to DVI, and interfaces to all major video processors. A S/PDIF port can output PCM encoded data as well as Dolby Digital, DTS and all other formats capable of being sent over S/PDIF. A 2-channel I2S port outputs data converted from S/PDIF. The SiI 9993 comes pre-programmed with HDCP keys, greatly simplifying the manufacturing process, lowering costs, all the while providing the highest level of HDCP key security. Silicon Image's PanelLink receivers use the latest generation of PanelLink TMDS core technology. These PanelLink cores pass all HDMI compliancy tests.

15.20.2. Features

• HDMI 1.0 and DVI 1.0 compliant receiver
• Integrated PanelLink core supports DTV resolutions (480i/576i/480p/576p/720p/1080i)
• Digital video interface supports video processors:
    o 24-bit RGB 4:4:4
    o 24-bit YCbCr 4:4:4
    o 16/20/24-bit YCbCr 4:2:2
    o 8/10/12-bit YCbCr 4:2:2 embedded syncs
• Analog RGB and YPbPr output:
    o 10-bit DAC
    o Separate or Composite Syncs (Sync on G)

• S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-48kHz Fs) using IEC 60958 and IEC 61937.
• Programmable I^2S interface for connection to low-cost audio DACs.
• Integrated HDCP decryption engine for receiving protected audio and video content
• Pre-programmed HDCP keys provide highest level of key security, simplifies manufacturing
• Programmable registers via slave I^2C interface
• 3.3V operation in 100-pin TQFP package
• Flexible power management

15.21. SN74CB3Q3305

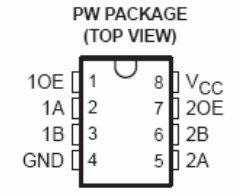
15.21.1. General Description

The SN74CB3Q3305 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3305 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

15.21.2. Features

• High-Bandwidth Data Path (Up To 500 MHz)
• 5-V Tolerant I/Os with Device Powered-Up or Powered-Down
• Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 3 Ω Typical)
• Rail-to-Rail Switching on Data I/O Ports
  − 0- to 5-V Switching With 3.3-V VCC
  − 0- to 3.3-V Switching With 2.5-V VCC
• Bidirectional Data Flow, With Near-Zero Propagation Delay
• Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)
• Fast Switching Frequency (f_{OE} = 20 MHz Max)
• Data and Control Inputs Provide Undershoot Clamp Diodes
• Low Power Consumption (ICC = 0.25 mA Typical)
• VCC Operating Range From 2.3 V to 3.6 V
• Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
• Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
• I_{off} Supports Partial-Power-Down Mode Operation
• Latch-Up Performance Exceeds 100 mA PerJESD 78, Class II
• ESD Performance Tested Per JESD 22
  − 2000-V Human-Body Model (A114-B, Class II)
  − 1000-V Charged-Device Model (C101)
• Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating

15.21.3. Pin Connections



15.22. ST24LC21

15.22.1. Description

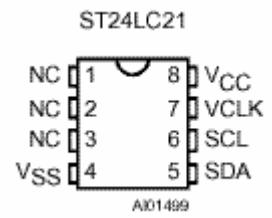
The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits. This device can operate in two modes: Transmit Only mode and I^2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I^2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The

ST24LC21 can not switch from the I²C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

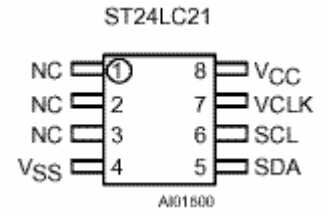
15.22.2. Features

• 1 million Erase/Write cycles
• 40 years data retention
• 2.5V to 5.5V single supply voltage
• 400k Hz compatibility over the full range of supply voltage
• Two wire serial interface I²C bus compatible
• Page Write (Up To 8 Bytes)
• Byte, random and sequential read modes
• Self timed programming cycle
• Automatic address incrementing
• Enhanced ESD/Latch up
• Performances

15.22.3. Pin connections



DIP Pin connections



CO Pin connections

NC: Not connected

Signal names

SDA	Serial data Address Input/Output
SCL	Serial Clock (I²C mode)
V_{cc}	Supply voltage
V_{ss}	Ground
VCLK	Clock transmit only mode

15.23. LM2576

15.23.1. General Description

The LM2576 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step–down switching regulator (buck converter). All circuits of this series are capable of driving a 3.0 A load with excellent line and load regulation.
These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version. These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2576 are offered by several different inductor manufacturers.
Since the LM2576 converter is a switch–mode power supply, its efficiency is significantly higher in comparison with popular three–terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated is so low that no heatsink is required or its size could be reduced dramatically.
A standard series of inductors optimized for use with the LM2576 are available from several different manufacturers. This feature greatly simplifies the design of switch–mode power supplies.
The LM2576 features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency (±2% over 0°C to 125°C). External shutdown is included, featuring 80 mA (typical) standby current. The output switch includes cycle–by–cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

15.23.2. Features

• 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions

• Adjustable Version Output Voltage Range, 1.23 to 37 V ±4% Maximum Over Line and Load Conditions
• Guaranteed 3.0 A Output Current
• Wide Input Voltage Range
• Requires Only 4 External Components
• 52 kHz Fixed Frequency Internal Oscillator
• TTL Shutdown Capability, Low Power Standby Mode
• High Efficiency
• Uses Readily Available Standard Inductors
• Thermal Shutdown and Current Limit Protection
• Moisture Sensitivity Level (MSL) Equals 1

15.23.3. Pin description

Pin 1. V_{in}
2. Output
3. Ground
4. Feedback
5. $\overline{ON}$/OFF

15.24. MC34063

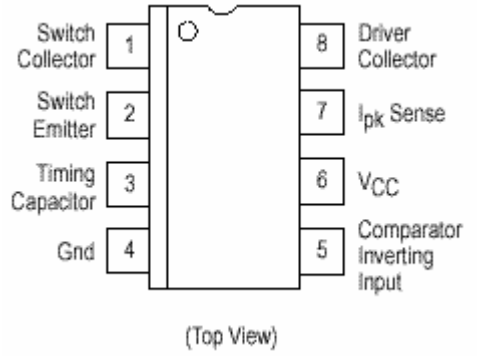
15.24.1. Description

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC–to–DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step–Down and Step–Up and Voltage–Inverting applications with a minimum number of external components.

15.24.2. Features

• Operation from 3.0 V to 40 V Input
• Low Standby Current
• Current Limiting
• Output Switch Current to 1.5 A
• Output Voltage Adjustable
• Frequency Operation to 100 kHz
• Precision 2% Reference

15.24.3. Pin connections



15.25. TDA1308

15.25.1. General Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

15.25.2. Features

• Wide temperature range
• No switch ON/OFF clicks
• Excellent power supply ripple rejection
• Low power consumption
• Short-circuit resistant
• High performance
• high signal-to-noise ratio
• High slew rate
• Low distortion
• Large output voltage swing.

15.25.3. Pinning

SYMBOL	PIN	DESCRIPTION	PIN VALUE
OUTA	1	Output A (Voltage swing)	Min : 0.75V, Max : 4.25V
INA(neg)	2	Inverting input A	Vo(clip) : Min : 1400mVrms
INA(pos)	3	Non-inverting input A	2.5V
V_{SS}	4	Negative supply	0V
INB(pos)	5	Non-inverting input B	2.5V
INB(neg)	6	Inverting input B	Vo(clip) : Min : 1400mVrms
OUTB	7	Output B (Voltage swing)	Min : 0.75V, Max : 4.25V
V_{DD}	8	Positive supply	5V, Min : 3.0V, Max : 7.0V

15.26. TDA9886

15.26.1. General Description

The TDA9886 is an alignment-free single standard (without positive modulation) vision and sound IF signal PLL.

15.26.2. Features

• 5 V supply voltage
• Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
• Multistandard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
• Gated phase detector for L/L accent standard
• Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative and positive modulated standards via I^2C-bus
• Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz
• 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
• VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
• Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analogue converter; AFC bits via I^2C -bus readable
• TakeOver Point (TOP) adjustable via I^2C-bus or alternatively with potentiometer
• Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by FM-PLL oscillator
• Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode (PLL controlled)
• SIF AGC for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I^2C-bus

• AM demodulator without extra reference circuit
• Alignment-free selective FM-PLL demodulator with high linearity and low noise
• I²C-bus control for all functions
• I²C-bus transceiver with pin programmable Module Address (MAD).

15.26.3. Pinning

SYMBOL	PIN	DESCRIPTION
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
OP1	3	output 1 (open-collector)
FMPLL	4	FM-PLL for loop filter
DEEM	5	de-emphasis output for capacitor
AFD	6	AF decoupling input for capacitor
DGND	7	digital ground
AUD	8	audio output
TOP	9	tuner AGC TakeOver Point (TOP)
SDA	10	I²C-bus data input/output
SCL	11	I²C-bus clock input
SIOMA	12	sound intercarrier output and MAD select
n.c.	13	not connected
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference input
VAGC	16	VIF-AGC for capacitor; note 1
CVBS	17	video output
AGND	18	analog ground
VPLL	19	VIF-PLL for loop filter
V_P	20	supply voltage (+5 V)
AFC	21	AFC output
OP2	22	output 2 (open-collector)
SIF1	23	SIF differential input 1
SIF2	24	SIF differential input 2

15.27. TPA3004D2

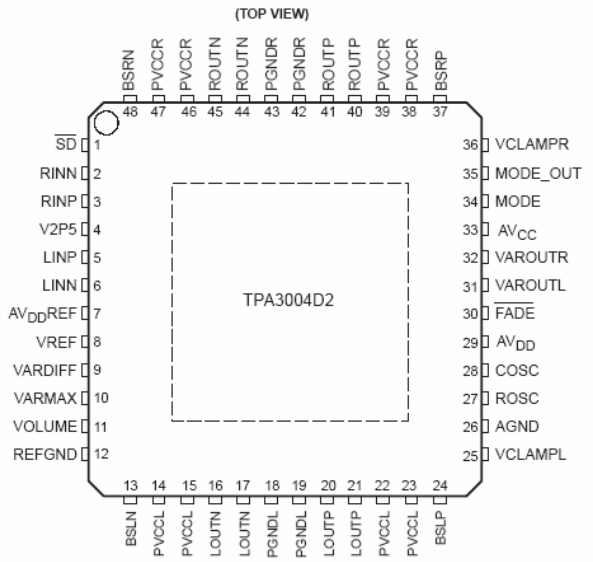
15.27.1. General Description

The TPA3004D2 is a 12-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3004D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3004D2 eliminates the need for external heatsinks when playing music.
Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from –40 dB to 36 dB. Line outputs, for driving external headphone amplifier inputs, are also dc voltage controlled with a range of gain from –56 dB to 20 dB.
An integrated 5-V regulated supply is provided for powering an external headphone amplifier.

15.27.2. Features

• 12-W/Ch Into an 8-Ω Load From 15-V Supply
• Efficient, Class-D Operation Eliminates Heatsinks and Reduces Power Supply Requirements
• 32-Step DC Volume Control From −40 dB to 36 dB
• Line Outputs For External Headphone Amplifier With Volume Control
• Regulated 5-V Supply Output for Powering TPA6110A2
• Space-Saving, Thermally-Enhanced PowerPAD™ Packaging
• Thermal and Short-Circuit Protection.

15.27.3. Pinning



TERMINAL NO.	NAME	I/O	DESCRIPTION
AGND	26	–	Analog ground for digital/analog cells in core
AV_{CC}	33	–	High-voltage analog power supply (8.5 V to 18 V)
AV_{DD}	29	O	5-V Regulated output capable of 100-mA output
AV_{DD}REF	7	O	5-V Reference output—provided for connection to adjacent VREF terminal.
BSLN	13	I/O	Bootstrap I/O for left channel, negative high-side FET
BSLP	24	I/O	Bootstrap I/O for left channel, positive high-side FET
BSRN	48	I/O	Bootstrap I/O for right channel, negative high-side FET
BSRP	37	I/O	Bootstrap I/O for right channel, positive high-side FET
COSC	28	I/O	I/O for charge/discharging currents onto capacitor for ramp generator triangle wave biased at V2P5
$\overline{FADE}$	30	I	Input for controlling volume ramp rate. A logic low on this pin places the amplifier in fade mode. A logic high on this pin allows a quick transition to the desired volume setting when cycling $\overline{SD}$ or during power-up.
LINN	6	I	Negative differential audio input for left channel
LINP	5	I	Positive differential audio input for left channel
LOUTN	16, 17	O	Class-D 1/2-H-bridge negative output for left channel
LOUTP	20, 21	O	Class-D 1/2-H-bridge positive output for left channel
MODE	34	I	Input for MODE control. A logic high on this pin places the amplifier in the variable output mode and the Class-D outputs are disabled. A logic low on this pin places the amplifier in the Class-D mode and Class-D stereo outputs are enabled. Variable outputs (VAROUTL and VAROUTR) are still enabled in Class-D mode to be used as line-level outputs for external amplifiers.
MODE_OUT	35	O	Output for control of the variable output amplifiers. When the MODE pin (34) is a logic high, the MODE_OUT pin is driven low. When the MODE pin (34) is a logic low, the MODE_OUT pin is driven high. This pin is intended for MUTE control of an external headphone amplifier. Leave unconnected when not used for headphone amplifier control.
PGNDL	18, 19	–	Power ground for left channel H-bridge
PGNDR	42, 43	–	Power ground for right channel H-bridge
PVCCL	14, 15	–	Power supply for left channel H-bridge (tied to pins 22 and 23 internally), not connected to PVCCR or AV_{CC}.
PVCCL	22, 23	–	Power supply for left channel H-bridge (tied to pins 14 and 15 internally), not connected to PVCCR or AV_{CC}.
PVCCR	38,39	–	Power supply for right channel H-bridge (tied to pins 46 and 47 internally), not connected to PVCCL or AV_{CC}.
PVCCR	46, 47	–	Power supply for right channel H-bridge (tied to pins 38 and 39 internally), not connected to PVCCL or AV_{CC}.
REFGND	12	–	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.
RINP	3	I	Positive differential audio input for right channel
RINN	2	I	Negative differential audio input for right channel
ROSC	27	I/O	Current setting resistor for ramp generator. Nominally equal to 1/8*V_{CC}
ROUTN	44, 45	O	Class-D 1/2-H-bridge negative output for right channel
ROUTP	40, 41	O	Class-D 1/2-H-bridge positive output for right channel
$\overline{SD}$	1	I	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to V_{CC}.
VARDIFF	9	I	DC voltage to set the difference in gain between the Class-D and VAROUT outputs. Connect to GND or AV_{DD}REF if VAROUT outputs are unconnected.
VARMAX	10	I	DC voltage that sets the maximum gain for the VAROUT outputs. Connect to GND or AV_{DD}REF if VAROUT outputs are unconnected.
VAROUTL	31	O	Variable output for left channel audio. Line level output for driving external HP amplifier.

VAROUTR	32	O	Variable output for right channel audio. Line level output for driving external HP amplifier.
VCLAMPL	25	–	Internally generated voltage supply for left channel bootstrap capacitors.
VCLAMPR	36	–	Internally generated voltage supply for right channel bootstrap capacitors.
VOLUME	11	I	DC voltage that sets the gain of the Class-D and VAROUT outputs.
VREF	8	I	Analog reference for gain control section.
V2P5	4	O	2.5-V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.
—	Thermal Pad	–	Connect to AGND and PGND—should be center point for both grounds.

15.28.

15.29. µPA672T

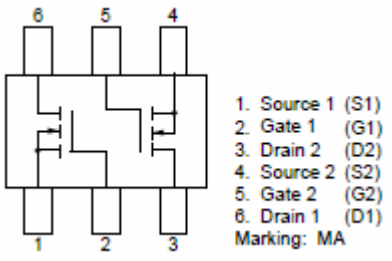
15.29.1. General Description

The µPA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

15.29.2. Features

• Two MOS FET circuits in package the same size as SC-70
• Automatic mounting supported

15.29.3. Pin Connection



1. Source 1 (S1)
2. Gate 1 (G1)
3. Drain 2 (D2)
4. Source 2 (S2)
5. Gate 2 (G2)
6. Drain 1 (D1)

Marking: MA

15.30. VPC3230D

15.30.1. General Description

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.
The main features of the VPC 323xD are
• high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
• multi-standard colour decoder PAL/NTSC/SECAM including all substandards
• four CVBS, one S-VHS input, one CVBS output
• two RGB/$YC_r C_b$ component inputs, one Fast Blank (FB) input
• integrated high-quality A/D converters and associated clamp and AGC circuits
• multi-standard sync processing
• linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ‘Panorama-vision’
• PAL+ preprocessing
• line-locked clock, data and sync, or 656-output interface
• peaking, contrast, brightness, color saturation and tint for RGB/ $YC_r C_b$ and CVBS/ S-VHS
• high-quality soft mixer controlled by Fast Blank
• PIP processing for four picture sizes (1/4, 1/9, 1/16 or 1/36 of normal size) with 8-bit resolution
• 15 predefined PIP display configurations and expert mode (fully programmable)
• control interface for external field memory
• I^2C-bus interface

• one 20.25-MHz crystal, few external components

• 80-pin PQFP package

15.30.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram
SUPPLYA = 4.75...5.25 V, SUPPLYD = 3.15...3.45 V

Pin No. PQFP 80-pin	Pin Name	Type	Connection (if not used)	Short Description
1	B1/CB1IN	IN	VREF	Blue1/Cb1 Analog Component Input
2	G1/Y1IN	IN	VREF	Green1/Y1 Analog Component Input
3	R1/CR1IN	IN	VREF	Read1/Cr1 Analog Component Input
4	B2/CB2IN	IN	VREF	Blue2/Cb2 Analog Component Input
5	G2/Y2IN	IN	VREF	Green2/Y2 Analog Component Input
6	R2/CR2IN	IN	VREF	Read2/Cr2 Analog Component Input
7	ASGF		X	Analog Shield GND_F
8	FFRSTWIN	IN	LV or GND_D	FIFO Reset Write Input
9	V_{SUPCAP}	OUT	X	Digital Decoupling Circuitry Supply Voltage
10	V_{SUPD}	SUPPLYD	X	Supply Voltage, Digital Circuitry
11	GND_D	SUPPLYD	X	Ground, Digital Circuitry
12	GND_{CAP}	OUT	X	Digital Decoupling Circuitry GND
13	SCL	IN/OUT	X	I^2C Bus Clock
14	SDA	IN/OUT	X	I^2C Bus Data
15	RESQ	IN	X	Reset Input, Active Low
16	TEST	IN	GND_D	Test Pin, connect to GND_D
17	VGAV	IN	GND_D	VGAV Input
18	YCOEQ	IN	GND_D	Y/C Output Enable Input, Active Low
19	FFIE	OUT	LV	FIFO Input Enable
20	FFWE	OUT	LV	FIFO Write Enable
21	FFRSTW	OUT	LV	FIFO Reset Write/Read
22	FFRE	OUT	LV	FIFO Read Enable
23	FFOE	OUT	LV	FIFO Output Enable
24	CLK20	IN/OUT	LV	Main Clock output 20.25 MHz
25	GND_{PA}	OUT	X	Pad Decoupling Circuitry GND
26	V_{SUPPA}	OUT	X	Pad Decoupling Circuitry Supply Voltage
27	LLC2	OUT	LV	Double Clock Output
28	LLC1	IN/OUT	LV	Clock Output
29	V_{SUPLLC}	SUPPLYD	X	Supply Voltage, LLC Circuitry
30	GND_{LLC}	SUPPLYD	X	Ground, LLC Circuitry
31	Y7	OUT	GND_Y	Picture Bus Luma (MSB)
32	Y6	OUT	GND_Y	Picture Bus Luma
33	Y5	OUT	GND_Y	Picture Bus Luma
34	Y4	OUT	GND_Y	Picture Bus Luma
35	GND_Y	SUPPLYD	X	Ground, Luma Output Circuitry
36	V_{SUPY}	SUPPLYD	X	Supply Voltage, Luma Output Circuitry
37	Y3	OUT	GND_Y	Picture Bus Luma
38	Y2	OUT	GND_Y	Picture Bus Luma
39	Y1	OUT	GND_Y	Picture Bus Luma
40	Y0	OUT	GND_Y	Picture Bus Luma (LSB)
41	C7	OUT	GND_C	Picture Bus Chroma (MSB)
42	C6	OUT	GND_C	Picture Bus Chroma
43	C5	OUT	GND_C	Picture Bus Chroma
44	C4	OUT	GND_C	Picture Bus Chroma
45	V_{SUPC}	SUPPLYD	X	Supply Voltage, Chroma Output Circuitry
46	GND_C	SUPPLYD	X	Ground, Chroma Output Circuitry
47	C3	OUT	GND_C	Picture Bus Chroma
48	C2	OUT	GND_C	Picture Bus Chroma
49	C1	OUT	GND_C	Picture Bus Chroma
50	C0	OUT	GND_C	Picture Bus Chroma (LSB)
51	GND_{SY}	SUPPLYD	X	Ground Sync Pad Circuitry
52	V_{SUPSY}	SUPPLYD	X	Supply Voltage, Sync Pad Circuitry
53	INTLC	OUT	LV	Interlace Output
54	AVO	OUT	LV	Active Video Output
55	FSY/HC/HSYA	OUT	LV	Front Sync/ Horizontal Clamp Pulse/Front-End Horizontal Sync Output
56	MSY/HS	IN/OUT	LV	Main Sync/Horizontal Sync Pulse
57	VS	OUT	LV	Vertical Sync Pulse
58	FPDAT/VSYA	IN/OUT	LV	Front End/Back-End Data/Front-End Vertical Sync Output
59	V_{STBYY}	SUPPLYA	X	Standby Supply Voltage
60	CLK5	OUT	LV	CCU 5 MHz Clock Output

61	NC	-	LV or GND_D	Not Connected
62	XTAL1	IN	X	Analog Crystal Input
63	XTAL2	OUT	X	Analog Crystal Output
64	ASGF		X	Analog Shield GND_F
65	GND_F	SUPPLYA	X	Ground, Analog Front-End
66	VRT	OUTPUT	X	Reference Voltage Top, Analog
67	I2CSEL	IN	X	I^2C Bus Address Select
68	ISGND	SUPPLYA	X	Signal Ground for Analog Input, connect to GND_F
69	V_{SUPF}	SUPPLYA	X	Supply Voltage, Analog Front-End
70	VOUT	OUT	LV	Analog Video Output
71	CIN	IN	LV	Chroma/Analog Video 5 Input
72	VIN1	IN	VRT	Video 1 Analog Input
73	VIN2	IN	VRT	Video 2 Analog Input
74	VIN3	IN	VRT	Video 3 Analog Input
75	VIN4	IN	VRT	Video 4 Analog Input
76	V_{SUPAI}	SUPPLYA	X	Supply Voltage, Analog Component Inputs Front-End
77	GND_{AI}	SUPPLYA	X	Ground, Analog Component Inputs Front-End
78	VREF	OUTPUT	X	Reference Voltage Top, Analog Component Inputs Front-End
79	FB1IN	IN	VREF	Fast Blank Input
80	AISGND	SUPPLYA	X	Signal Ground for Analog Component Inputs, connect to GND_{AI}

15.31. MAD4868A

15.31.1. General Description

The Micronas Audio Delay IC MAD 4868A acts as a delay line for TV audio and consumer audio applications. The IC is designed for synchronizing audio and video signals ensuring "Lip Sync" by delaying the audio signal with the same amount of time as the video signal is delayed in a TV's video processing.

For TV designs, independent signals for loudspeakers, headphones, and line-out or S/PDIF out must be provided, resulting in the need to delay six independent audio channels.

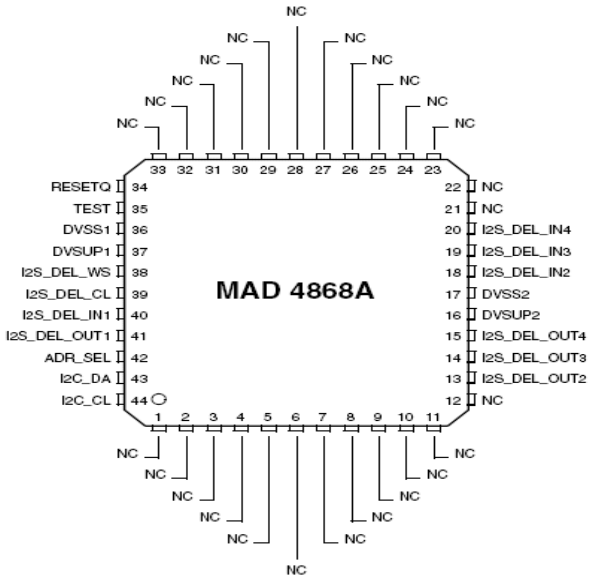
15.31.2. Features

- 32 k audio samples RAM:
- Total delay time of 680 ms at 48 kHz or 1020 ms at 32 kHz sampling rate
- 32/18-bit word width:
- 32-bit High-Resolution mode or 18-bit Standard mode
- Sampling rates from 32 kHz to 48 kHz for serial 8-channel mode are supported
- Sampling rates from 4 kHz to 192 kHz for parallel 2-channel mode are supported
- Memory allocation:
- MAD 4868A's memory can be allocated for 1... 8 audio channels. Delay time can be programmed for each channel individually.

15.31.3. Interfaces

- 8-channel Micronas I^2S input and output:
- In combination with Micronas ICs (serial mode) (e.g. MSP 44/46xyK, MAS 35xyH), eight audio channels can be routed through MAD 4868A by using four lines only.
- 4x2-channel standard I^2S inputs and outputs (paral lel mode) allow routing eight audio channels with sampling rates of 4... 192 kHz through MAD 4868A
- I^2C control for delay time programming
- Address select to set one out of two available I^2C addresses.

15.31.4. Pinning



Pin No. PMQFP44-1	Pin Name	Type	Connection (If not used)	Short Description
1...12	NC		LV	Not Connected
13	I2S_DEL_OUT2	OUT	OBL	I^2S data output channel 3 + 4
14	I2S_DEL_OUT3	OUT	OBL	I^2S data output channel 5 + 6
15	I2S_DEL_OUT4	OUT	OBL	I^2S data output channel 7 + 8
16	DVSUP2	SUP	DVSUP	Digital Power Supply
17	DVSS2	SUP	DVSS	Digital Ground
18	I2S_DEL_IN2	IN	OBL	I^2S data input channel 3 + 4
19	I2S_DEL_IN3	IN	OBL	I^2S data input channel 5 + 6
20	I2S_DEL_IN4	IN	OBL	I^2S data input channel 7 + 8
21...33	NC		LV	Not Connected
34	RESETQ	IN	OBL	Power-On Reset (active low)
35	TEST	IN	DVSS	Test pin
36	DVSS1	SUP	DVSS	Digital Ground
37	DVSUP1	SUP	DVSUP	Digital Power Supply
38	I2S_DEL_WS	IN	OBL	I^2S word strobe input
39	I2S_DEL_CL	IN	OBL	I^2S clock input
40	I2S_DEL_IN1	IN	OBL	I^2S data input channel 1 + 2 or 1..8
41	I2S_DEL_OUT1	OUT	OBL	I^2S data output channel 1 + 2 or 1..8
42	ADR_SEL	IN	OBL	I^2C bus address select
43	I2C_DA	IN/OUT	OBL	I^2C Data
44	I2C_CL	IN/OUT	OBL	I^2C Clock

15.32. SVP-EX 59B

General Description

To improve the video quality of the PAL CVBS and HD video input, the all layer changed EX59 improve video sharpness function in HD channel and enhance the 3D PAL quality compared to EX52 Rev. D chips.

16. SERVICE MENU SETTINGS

To enter the service menu, first enter the MENU by pressing "▣" button and then press the digits 4, 7, 2 and 5 respectively.

16.1. Picture Adjust

- *Source => All possible sources given with the chasis as a list.*
- *Mode => Three items as a list; NATURAL, DYNAMIC, CINEMA*
- *Colour Temp => Three items as a list; COOL, NORMAL, WARM*
- *Contrast => Slider Bar. Changing value between 0 to 63.*
- *Brightness => Slider Bar. Changing value between 0 to 63.*
- *Sharpness => Slider Bar. Changing value between 0 to 16.*
- *Colour => Slider Bar. Changing value between 0 to 99.*
- *R => Slider Bar. Changing value between 0 to 100.*
- *G => Slider Bar. Changing value between 0 to 100.*
- *B => Slider Bar. Changing value between 0 to 100.*

In this menu preset values for each Mode (Contrast, Brightness, Sharpness, Colour values for each Mode- NATURAL, DYNAMIC, CINEMA) and for each Colour Temp. (R, G, B values for each Colour Temp- COOL, NORMAL, WARM) are determined for each source.

16.2. SOUND1

- *Menu Subwoofer => If ON, Subwoofer option is available in TV set, and the item is visible in sound menu, else Subwoofer is not available.*
- *Subwoofer Level (dB) => This value is gain value of Subwoofer output in dB. -30...12*
- *Subwoofer Corner Freq. (x10Hz) => Last low frequency value that is amplified. 5...40*
- *Menu Dolby Prologic => No functionality now.*
- *Menu Equalizer => If ON, visible in sound menu, else invisible.*
- *Menu Lineout => No functionality now.*
- *Menu Headphone => If ON, visible in sound menu, else invisible.*
- *Menu Hyper Sound => If ON, visible in sound menu, else invisible.*
- *Menu Wide Sound => If ON, visible in sound menu, else invisible.*
- *Menu Dynamic Bass => If ON, visible in sound menu, else invisible.*
- *Menu Virtual Dolby => If ON, visible in sound menu, else invisible.*
- *Carrier Mute => If ON, in the absence of an FM carrier the output is muted, else not.*
- *Virtual Dolby Text => Active if VIRTUAL DOLBY is ON. According to the selection; seen in sound menu as 3D PANORAMA or VIRTUAL DOLBY.*

16.3. SOUND 2

- *AVL => AVL is controlled from this menu by service user. ON/OFF*
- *Menu AVL => If ON, AVL item is visible in sound menu, and AVL can be controlled from sound menu by normal user, else AVL is invisible to normal user.*
- *FM PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for the related standard. 0...127*
- *NICAM PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for the related standard. 0...127*
- *SCART PRESCALE AVL ON => If AVL ON, set value in this item is used as prescale value for scart outputs. 0...127*
- *SCART VOLUME AVL ON => If AVL ON, set value in this item is used as volume value for scart1 and scart2. 0...127*
- *FM PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127*
- *NICAM PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for the related standard. 0...127*
- *SCART PRESCALE AVL OFF => If AVL OFF, set value in this item is used as prescale value for scart outputs. 0...127*
- *SCART VOLOUME AVL OFF => If AVL OFF, set value in this item is used as volume value for scart1 and scart2. 0...127*

16.4. Options

- *Screen Saver =>*
- *FIRST APS => If ON, first APS menu is opened when the TV opened with the factory default settings.*

- *APS VOLUME => After First APS function finishes, the volume of the TV is that value.*
- *AGC => Tuner AGC value.*
- *Factory Reset => OK to activate. When OK pressed on this item, factory defaults loaded.*
- *Enter Flash Mode =>*

TV Norm

- *BG => If ON, supported, else not supported*
- *DK => If ON, supported, else not supported.*
- *I => If ON, supported, else not supported.*
- *L => If ON, supported, else not supported.*
- *LP => If ON, supported, else not supported.*
- *M => If ON, supported, else not supported.*

Features

- *PIP/PAP => If ON, PIP/PAP available else not.*
- *Blue Background => If ON, Blue Background is visible in Features Menu else not.*
- *Menu Transparency => If ON, Menu Transparency is visible in Features Menu else not.*
- *Menu Timeout => If ON, Menu Timeout is visible in Features Menu else not.*
- *Backlight => If ON, Backlight is visible in Features Menu else not.*
- *Single Tuner =>*

Teletext

- *Teletext Language => Teletext Language may be controlled from this menu by service user.*
- *Menu Teletext Language => If ON, Teletext Language item is visible in Features Menu, and Teletext Language can be controlled from Features Menu by normal user, else Teletext Language is invisible to normal user.*

Source

- *TV*
- *SC1*
- *SC2*
- *SC2 SVHS*
- *SC3*
- *SC3 SVHS*
- *YPBPR*
- *FAV*
- *SVHS*
- *HDMI*
- *PC*

This menu is related with the options of the chassis. These items may be ON or OFF. If ON, the source is available in TV set, and the item is visible in source menu, else the source may be available but invisible to user.

17. IC DESCRIPTIONS (FOR DIGITAL)

STI5518	24C32
MAX232_SMD	STV0360
74HCU04	MAX809
TSH22	TDCC2345TV39A
CS4334	STV0700
AMIC A43L2616	
MX29LV160T	

17.1. STI5518

17.1.1. General Description

The STi5518 is a highly integrated single-chip decoder, designed for use in feature-rich mass-market set-top boxes. It integrates a high-performance 32-bit CPU, a dedicated block for DVB/DirecTV transport demultiplexing and descrambling, modules for MPEG-2 video and audio decoding with 3D-surround and MP3 support, advanced display and graphics features, a digital video encoder and all of the system peripherals required in a typical low-cost interactive receiver.

To cover the needs of DVD-capable set-top boxes, STi5518 integration options include a CSS decryption block, a Dolby Digital audio decoder and Macrovision copy protection.
An ATAPI interface is built-in, supporting the glueless connection of standard Hard Disk Drives. In this way, the STi5518 is ideal for set-top boxes featuring trick modes such as live TV recording, pausing and time-shifting.
The STi5518 is backward compatible with the popular STi5500 set-top box decoder, allowing easy migration from the previous generation.
The high level of integration in a single PQFP-208 package makes the STi5518 ideally suited for low-cost, high-volume set-top box applications.

17.2. MAX232_SMD

17.2.1. General Description

The MAX220–MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, particularly applications where ±12V is not available.
These parts are especially useful in battery-powered systems, since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX225, MAX233, MAX235, and MAX245/MAX246/MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

17.2.2. Features

- Operate from Single +5V Power Supply (+5V and +12V—MAX231/MAX239)
- Low-Power Receive Mode in Shutdown (MAX223/MAX242)
- Meet All EIA/TIA-232E and V.28 Specifications
- Multiple Drivers and Receivers
- 3-State Driver and Receiver Outputs
- Open-Line Detection (MAX243)

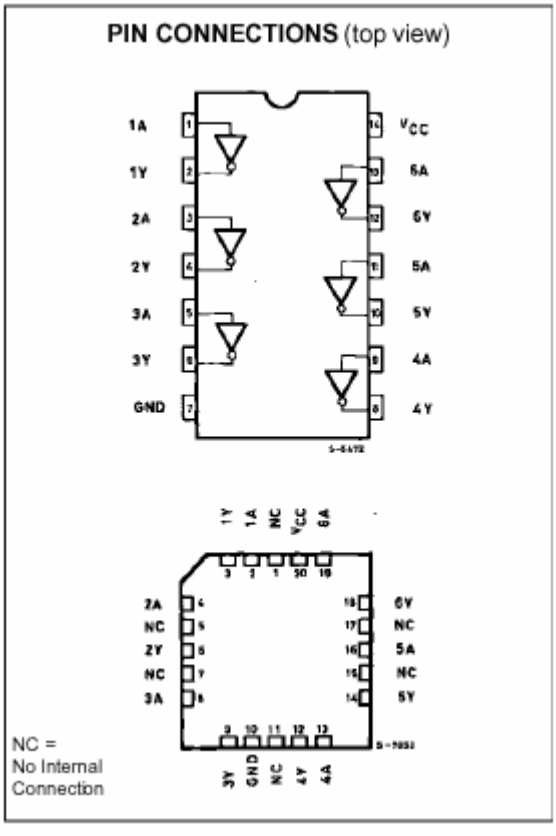
17.3. 74HCU04

17.3.1. General Description

The M54/74HCU04 is a high speed CMOS HEX INVERTER (SINGLE STAGE) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
As the internal circuit is composed of a single stage inverter, it can be used in crystal oscillator.
All inputs are equipped with circuits against static discharge and transient excess voltage.

17.3.2. Pin Description

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

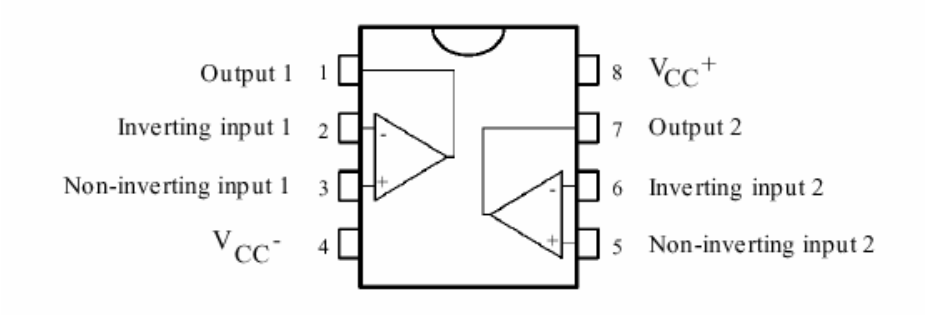


17.4. TSH22

17.4.1. General Description

The TSH22 is a dual bipolar operational amplifier offering a single supply operation from 3V to 30V with very good performances: medium speed (25MHz), unity gain stability and low noise.
The TSH 22 is therefore an enhanced replacement of standard dual operational amplifiers.

17.4.2. Pin Connections



17.5. CS4334

17.5.1. General Description

The CS4334 family members are complete, stereo digital-to-analogue output systems including interpolation, 1-bit D/A conversion and output analogue filtering in an 8-pin package. The CS4334/5/6/7/8/9 support all major audio data interface formats and the individual devices differ only in the supported interface format.
The CS4334 family is based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analogue low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.
The CS4334 family contains on-chip digital de-emphasis, operates from a single +5V power supply, and requires minimal support circuitry. These features are ideal for portable CD players and other portable playback systems.

17.5.2. Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analogue Filtering
- 24-Bit Conversion
- 96 dB Dynamic Range
- Low Distortion
- Low Clock Jitter Sensitivity
- Single 5 V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis
- Soft Ramp to Quiescent Output Voltage
- Functionally Compatible with CS4330/31/33

17.6. AMIC A43L2616

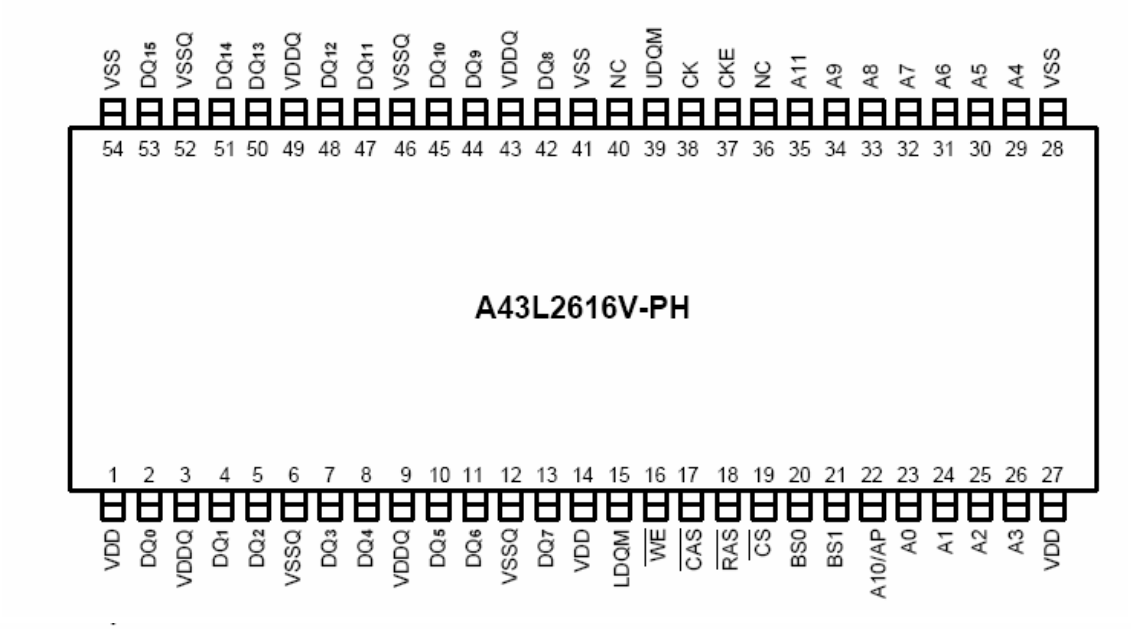
17.6.1. General Description

The A43L2616-PH is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 X 1,048,576 words by 16 bits, fabricated with AMIC's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

17.6.2. Features

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks / Pulse RAS
- MRS cycle with address key programs

- All inputs are sampled at the positive going edge of the system clock
- Clock Frequency: 166MHz @ CL=3
  143MHz @ CL=3
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)
- 54 Pin TSOP (II)



Symbol	Name	Description
CLK	System Clock	Active on the positive going edge to sample all inputs.
$\overline{CS}$	Chip Select	Disables or Enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one clock + tss prior to new command. Disable input buffers for power down in standby.
A0~A11	Address	Row / Column addresses are multiplexed on the same pins. Row address : RA0~RA11, Column address: CA0~CA7
BS0, BS1	Bank Select Address	Selects bank to be activated during row address latch time. Selects band for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and Row precharge.
L(U)DQM	Data Input/Output Mask	Makes data output Hi-Z, t SHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ_{0-15}	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power Supply/Ground	Power Supply: +3.3V±0.3V/Ground
VDDQ/VSSQ	Data Output Power/Ground	Provide isolated Power/Ground to DQs for improved noise immunity.
NC/RFU	No Connection	

17.7. MX29LV160T

17.7.1. General Description

The MX29LV160T/B & MX29LV160AT/AB is a 16-megabit Flash memory organized as 2M bytes of 8 bits or 1M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV160T/B & MX29LV160AT/AB is packaged in 44-pin SOP, 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

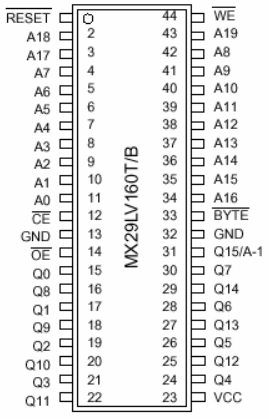
The standard MX29LV160T/B & MX29LV160AT/AB offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV160T/B &MX29LV160AT/AB has separate chip enable (CE) and output enable (OE) controls.
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV160T/B & MX29LV160AT/AB uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.
MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29LV160T/B & MX29LV160AT/AB uses a 2.7V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

17.7.2. Features

- Extended single - supply voltage range 2.7V to 3.6V
- 2,097,152 x 8/1,048,576 x 16 switchable
- Single power supply operation
- Fast access time: 70/90ns
- Low power consumption
- Command register architecture
- Auto Erase (chip & sector) and Auto Program
- Erase Suspend/Erase Resume
- Status Reply
- Ready/Busy pin (RY/BY)
- Sector protection
- CFI (Common Flash Interface) compliant (for MX29LV160AT/AB)
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Sector Architecture
- Low VCC write inhibit is equal to or less than 1.4V
- Compatibility with JEDEC standard

17.7.3. Pin Description

44 SOP(500 mil)



SYMBOL	PIN NAME
A0~A19	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{BYTE}$	Word/Byte Selection input
$\overline{RESET}$	Hardware Reset Pin/Sector Protect Unlock
$\overline{OE}$	Output Enable Input
RY/$\overline{BY}$	Ready/Busy Output
VCC	Power Supply Pin (2.7V~3.6V)
GND	Ground Pin

17.8. 24C32

17.8.1. General Description

The AT24C32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32/64 is available in space saving 8-pin JEDEC PDIP, 8-pin JEDEC SOIC, 8-pin EIAJ SOIC, and 8-pin TSSOP (AT24C64) packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

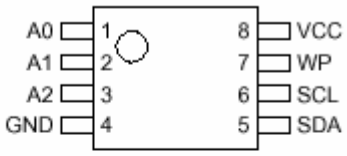
17.8.2. Features

- Low-Voltage and Standard-Voltage Operation
- Low-Power Devices (I_{SB}= 2 µA at 5.5V) Available
- Internally Organized 4096 x 8, 8192 x 8
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Clock Rate
- Write Protect Pin for Hardware Data Protection
- 32-Byte Page Write Mode (Partial Page Writes Allowed)
- Self-Timed Write Cycle (10 ms max)
- High Reliability
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC PDIP, 8-Pin JEDEC SOIC, 8-Pin EIAJ SOIC, and 8-pin TSSOP Packages

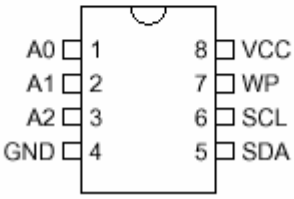
17.8.3. Pin Description

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

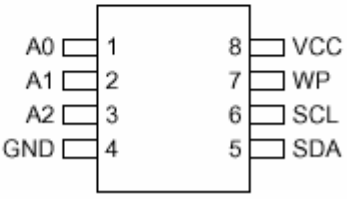
8-Pin TSSOP



8-Pin PDIP



8-Pin SOIC



SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.
SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.
DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). When the pins are not hardwired, the default A_2, A_1, and A_0 are zero.
WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the upper quadrant (8/16K bits) of memory are inhibited. If left unconnected, WP is internally pulled down to GND.

17.9. STV0360

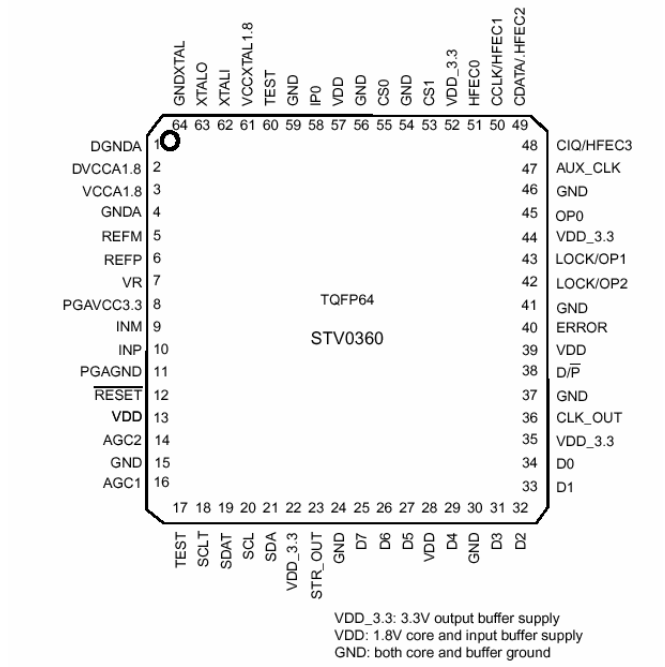
17.9.1. General Description

The STV0360 is a single-chip COFDM (coded orthogonal frequency division multiplex) demodulator that performs IF to MPEG-2 block processing of OFDM carriers. It is intended for digital terrestrial receivers for compressed video, sound and data services.
The chip implements all the functions from the tuner IF output up to the MPEG-2 transport stream input.
The STV0360 is fully compliant with the DVB-T specification (ETS 300 744) and handles 2K/8K modes.
The STV0360 integrates an A/D converter that delivers the required performance to handle up to 64 QAM carriers in a direct IF sampling architecture, thus eliminating the need for an external down-converter. The chip also integrates an internal programmable gain amplifier (PGA) to compensate for SAW filter level degradation, thus eliminating the need for external IF amplifiers. A 10-bit ADC, intended for RF signal strength indication, eliminates the need for external components when using wide-band AGC tuners.
In addition to all the demodulation and FEC (forward error correction) functions required for recovery of the QAM modulated bit streams with very low BER, it also includes several features that give easy and immediate access to various quality monitoring parameters or lock status. The STV0360 also provides output such as delayed AGC or noise-free I²C bus dedicated to tuner control, which facilitates the design of high quality integrated receiver decoders.
The STV0360 outputs error-corrected MPEG-2 transport streams and complies with the DVB common interface format, with programmable data clock frequency. It also interfaces seamlessly with the packet de-multiplexers embedded in the STi55xx Omega family of single-chip decoders.

17.9.2. Features

- Decodes DVB-T (ETS300744) and NorDig II
- TPS decoded or automatic FEC mode detection
- Embeds PGA for IF level adaptation
- Generates system clock on-chip from 20 to 27-MHz crystal quartz
- Four I²C addresses available
- Low power consumption (< 500 mW)
- Small footprint: TQFP64 (10 X 10 mm)
- 1.8 V operation, CMOS technology

17.9.3. Pin Description



Pin number	Name	Type	Description	Drive (mA)
Clock and resets				
12	$\overline{\text{RESET}}$	I[a]	Hardware reset, active low	-
62	XTALI	Analog	Crystal oscillator input/external clock (1.8 V)	-
63	XTALO	Analog	Crystal oscillator output	-
61	VCCXTAL1.8	Supply	Analog oscillator supply (1.8 V)	-
64	GNDXTAL	Ground	Analog oscillator ground	-
Analog interface				
2	DVCCA1.8	Supply	Analog part digital supply (1.8 V)	-
5	REFM	Analog	Internal negative reference	-
6	REFP	Analog	Internal positive reference	
3	VCCA1.8	Supply	Analog supply (1.8 V)	-
9	INM	Analog	Negative analog input	-
10	INP	Analog	Positive analog input	-
4	GNDA	Supply	Analog ground	-
1	DGNDA	Ground	Analog ground	-
7	VR	Analog	Reference	-
11	PGAGND	Supply	PGA ground	-
8	PGAVCC3.3	Supply	PGA VCC (3.3 V)	
I^2C interface				
21	SDA	IO[b]	Serial data (open drain)	8
20	SCL	I	Serial clock (open drain)	-
19	SDAT	IO	SDA tuner (open drain)	4
18	SCLT	I	SCL tuner	
MPEG interface				
25, 26, 27, 29, 31, 32, 33, 34	D7/0	O[c]	Serial D7, MPEG data	8/4
36	CLK_OUT	O	MPEG byte or bit clock	4
23	STR_OUT	O	MPEG first byte sync	2
38	D/$\overline{\text{P}}$	O	MPEG data valid/parity	4
40	ERROR	O	MPEG packet error	2
51	HFEC0	O	Hierarchical FEC output bit 0	2
50	CCLK/HFEC1	O	Hierarchical FEC output bit 1 or clock for constellation display	2
49	CDATA/HFEC2	O	Hierarchical FEC output bit 2 or data for constellation display	2
48	CIQ/HFEC3	O	Hierarchical FEC output bit 3 or IQ validation for constellation display	2

Front end controls

16	AGC1	IO	RF AGC control ΣΔ	4
14	AGC2	IO	IF AGC control ΣΔ	4
17, 60	TEST		Reserved test mode, must be grounded	
58	IP0	I	General purpose input port 0 and ADC input for RF level monitoring	-
45	OP0	IO	General purpose output port 0	4
43	LOCK/OP1	IO	General purpose output port 1 or lock indicator	4
42	LOCK/OP2	O	General purpose output port 2 or lock indicator	4
47	AUX_CLK	IO	Auxiliary clock	8
55	CS0	I	Chip select LSB	-
53	CS1	I	Chip select MSB	-

Power supply

13, 28, 39, 57	VDD	Supply	Digital core supply	
22, 35, 44, 52	VDD_3.3	Supply	Digital IO supply	
15, 24, 30, 37, 41, 46, 54, 56, 59	GND	Ground		

a. All inputs are 3.3 V compatible
b. All bidirectional pads are 3.3 V capable
c. All outputs are 3.3 V capable

17.10. MAX809

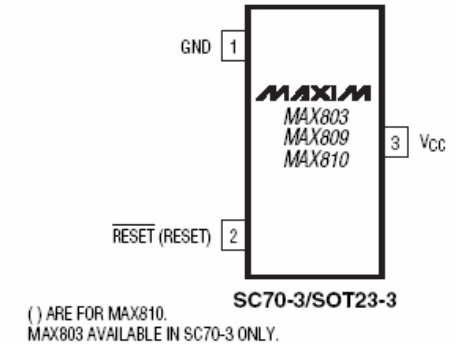
17.10.1. General Description

The MAX803/MAX809/MAX810 are microprocessor (µP) supervisory circuits used to monitor the power supplies in µP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V,+3.0V, or +2.5V powered circuits. These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available. The MAX803 has an open-drain output stage, while the MAX809/MAX810 have push-pull outputs. The MAX803's open-drain RESET output requires a pull-up resistor that can be connected to a voltage higher than V_{CC}. The MAX803/MAX809 have an active-low RESET output, while the MAX810 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1V. Low supply current makes the MAX803/MAX809/MAX810 ideal for use in portable equipment. The MAX803 is available in a 3-pin SC70 package, and the MAX809/MAX810 are available in 3-pin SC70 or SOT23 packages.

17.10.2. Features

- 1 Precision Monitoring of +2.5V, +3V, +3.3V, and +5V Power-Supply Voltages
- Fully Specified Over Temperature
- Available in Three Output Configurations
  Open-Drain RESET Output (MAX803)
  Push-Pull RESET Output (MAX809)
  Push-Pull RESET Output (MAX810)
- 140ms min Power-On Reset Pulse Width
- 12µA Supply Current
- Guaranteed Reset Valid to V_{CC} = +1V
- Power Supply Transient Immunity
- No External Components
- 3-Pin SC70 and SOT23 Packages

17.10.3. Pin Description



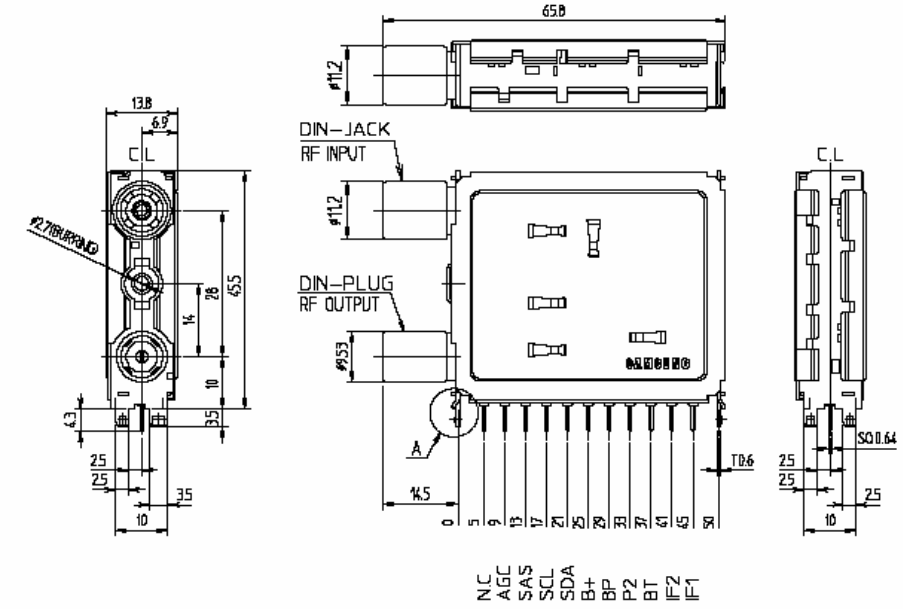
PIN	NAME	FUNCTION
1	GND	Ground
2	$\overline{\text{RESET}}$ (MAX803/ MAX809)	$\overline{\text{RESET}}$ Output remains low while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
	RESET (MAX810)	RESET Output remains high while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
3	V_{CC}	Supply Voltage (+5V, +3.3V, +3.0V, or +2.5V)

17.11. TDCC2345TV39A

17.11.1. General Description

- Receiving System : Designed to cover all bands in VHF and UHF including digital terrestrial channels for DVB-T system.
- Receiving Channel : 47 MHz ~ 862 MHz
- Intermediate Frequency : Digital (center) 36.125 MHz
- Input Impedance : 75Ω, Unbalanced.
- IF Output Impedance : 75Ω, Balanced.
- Loop through RF output Impedance : 75Ω, Unbalanced.
- Band Change-Over System : PLL system
- Tuning System : PLL system
- Pin-out for the port to control the switchable saw

17.11.2. Pin Description



PIN	CONNECTION
1	N.C
2	AGC
3	SAS
4	SCL
5	SDA
6	B+ (for preamp)
7	BP
8	P2 Port (For S/W)
9	BT
10	IFOUT2
11	IFOUT1
12	RF INPUT
13	RF OUTPUT

17.12. STV0700

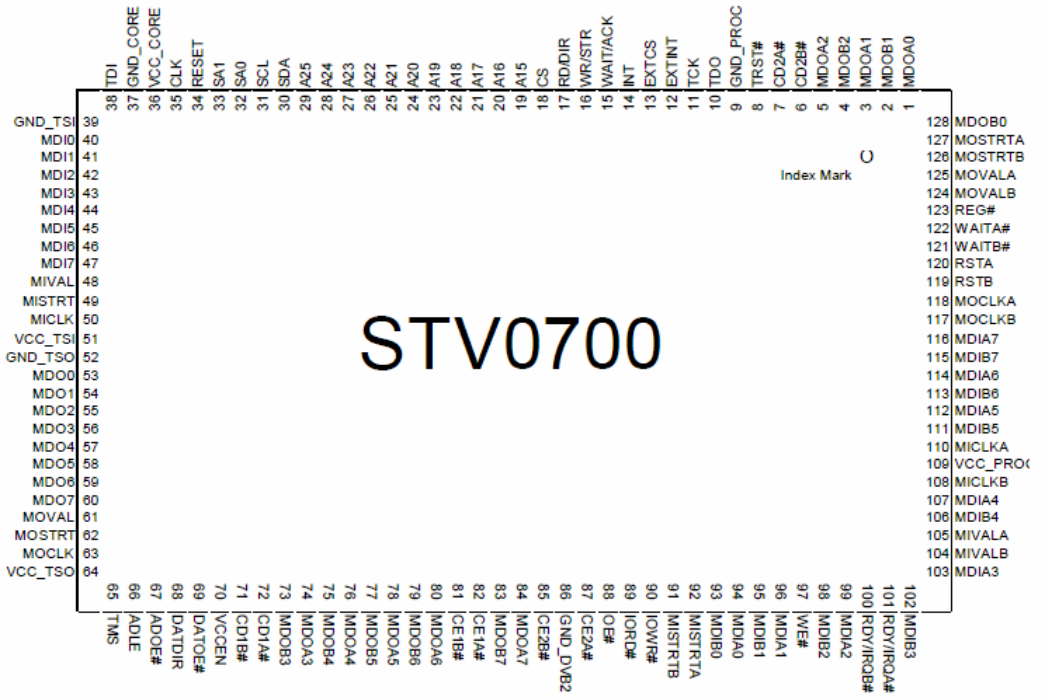
17.12.1. General description

The STV0700 controller contributes to offer an optimized, homogeneous and complete solution for digital TV receiver and Set Top Box manufacturers that want to quickly implement the Common Interface. The STV0700 includes the necessary I/Os to interface to the MPEG Transport stream generated by the receiver demodulator and daisy chain it through two independent Common Interface modules and back to the demultiplexer. The STV0700 interfaces with major digital TV receiver microprocessors. An I^2C bus is used for initialization and module selection, while a Universal Control Signal Generator (UCSG) maps CPU control bus into Command Interface control signals. To minimize pin count, host address and data buses transit through external buffers that are driven by the STV0700. The STV0700 includes a memory mode that allows the use any of the Common Interface slots to read and write an 8-bit PC Card Memory card. This feature gives the receiver memory extension capability for software upgrade or better performance.

17.12.2. Features

- Module Interface
  - 2 independent module capability
  - Common Interface Standard compliant
    - DVB_CI (CENELEC EN-50221)
    - NRSS-B (SCTE IS-679 Part B)
    - DAVIC v1.2 (CA0 interface)
  - Memory PCMCIA compliance (R2)
    - 8-bit data access
    - 26-bit address Memory Card
  - Attribute Memory access (CIS, Tupple)
  - High speed capability
    - Up to 20Mbits/s on Command Interface
    - Up to 100Mbits/s on Transport Stream
  - Polling and Interrupt modes
  - Hot Insertion (Automatic and Reset VCC handling)
  - 3.3V (5V tolerant) I/O buffers
- IEEE 1149.1 Boundary Scan Compliant
- Host microprocessor Interface
  - Universal Control Signal Generator(UCSG)
    - PC Card control signals generation
    - Supports PowerPC, ARM, ST20,68xxx, TMS, LSI 64008, TC81220F IDTR3041
  - I^2C port
    - STV0700 Set-up
    - Slot selection
    - Cascade mode management (up to 4STV0700)
  - Chip Select bank and Interrupt facilities
  - 3.3V (5V tolerant) I/O buffers
- Digital Video Stream Interface
- MPEG II Transport Stream compliant (serial/parallel configurable interface)
- 3.3V (5V tolerant) I/O buffer for direct interface with FEC and DEMUX ICs

17.12.3. Pin Description



Host microprocessor interface (24 pins)

Name	I/O	Type	RST	Function
RESET	I	TTL		STV0700 reset
CLK	I	TTL		27MHz clock input
SA1	I	TTL		I^2C address bit 2
SA0	I	TTL		I^2C address bit 1
SCL	I	TTL trig		I^2C clock
SDA	I/O	TTL trig	Z	I^2C data
A25	I	TTL		Host microprocessor address bit 25
A24	I	TTL		Host microprocessor address bit 24
A23	I	TTL		Host microprocessor address bit 23
A22	I	TTL		Host microprocessor address bit 22
A21	I	TTL		Host microprocessor address bit 21
A20	I	TTL		Host microprocessor address bit 20
A19	I	TTL		Host microprocessor address bit 19
A18	I	TTL		Host microprocessor address bit 18
A17	I	TTL		Host microprocessor address bit 17
A16	I	TTL		Host microprocessor address bit 16
A15	I	TTL		Host microprocessor address bit 15
CS	I	TTL		STV0700 chip select input
RD/DIR	I	TTL		Read strobe / transfer direction input
WR/STR	I	TTL		Write strobe / transfer strobe
WAIT/ACK	O	TTL 3-state	Z	WAIT / transfer acknowledge
INT	O	TTL 3-state	Z	Interrupt output to host microprocessor
EXTCS	O	TTL 3-state	Z	External device chip select
EXTINT	I	TTL		External device interrupt input

IEEE 1149.1 Interface (5 pins)

Name	I/O	Type	RST	Function
TCK	I	TTL trig		JTAG test clock
TMS	I	TTL up		JTAG test mode select
TDI	I	TTL up		JTAG test data in
TRST#	I	TTL up		JTAG test reset
TDO	O	TTL 3-state	Z	JTAG test data out

Host TS interface (22 pins)

Name	I/O	Type	RST	Function
MICLK	I	TTL		MPEG clock input from front-end
MISTRT	I	TTL		MPEG packet start input (scan in)
MIVAL	I	TTL		MPEG valid data input (scan enable)
MDI7	I	TTL		MPEG data input bit 7
MDI6	I	TTL		MPEG data input bit 6
MDI5	I	TTL		MPEG data input bit 5
MDI4	I	TTL		MPEG data input bit 4
MDI3	I	TTL		MPEG data input bit 3
MDI2	I	TTL		MPEG data input bit 2
MDI1	I	TTL		MPEG data input bit 1

MDI0	I	TTL		MPEG data input bit 0 (Serial data in)
MOCLK	O	TTL 3-state	0	MPEG clock output to MPEG decoder
MOSTRT	O	TTL 3-state	0	MPEG packet start output
MOVAL	O	TTL 3-state	0	MPEG valid data output
MDO7	O	TTL 3-state	0	MPEG data output bit 7
MDO6	O	TTL 3-state	0	MPEG data output bit 6
MDO5	O	TTL 3-state	0	MPEG data output bit 5
MDO4	O	TTL 3-state	0	MPEG data output bit 4
MDO3	O	TTL 3-state	0	MPEG data output bit 3
MDO2	O	TTL 3-state	0	MPEG data output bit 2
MDO1	O	TTL 3-state	0	MPEG data output bit 1
MDO0	O	TTL 3-state	0	MPEG data output bit 0 (Serial data out)

Modules TS interface (44 pins)

Name	I/O	Type	RST	Function
MICLKA	O	TTL 3-state	Z	Module A MPEG clock input
MISTRTA	O	TTL 3-state	Z	Module A MPEG packet start input
MIVALA	O	TTL 3-state	Z	Module A MPEG valid data input
MDIA7	O	TTL 3-state	Z	Module A MPEG data input bit 7
MDIA6	O	TTL 3-state	Z	Module A MPEG data input bit 6
MDIA5	O	TTL 3-state	Z	Module A MPEG data input bit 5
MDIA4	O	TTL 3-state	Z	Module A MPEG data input bit 4
MDIA3	O	TTL 3-state	Z	Module A MPEG data input bit 3
MDIA2	O	TTL 3-state	Z	Module A MPEG data input bit 2
MDIA1	O	TTL 3-state	Z	Module A MPEG data input bit 1
MDIA0	O	TTL 3-state	Z	Module A MPEG data input bit 0
MOCLKA	I	TTL		Module A MPEG clock output to MPEG decoder
MOSTRTA	I	TTL		Module A MPEG packet start output
MOVALA	I	TTL		Module A MPEG valid data output
MDOA7	I	TTL		Module A MPEG data output bit 7
MDOA6	I	TTL		Module A MPEG data output bit 6
MDOA5	I	TTL		Module A MPEG data output bit 5
MDOA4	I	TTL		Module A MPEG data output bit 4
MDOA3	I	TTL		Module A MPEG data output bit 3
MDOA2	I	TTL		Module A MPEG data output bit 2
MDOA1	I	TTL		Module A MPEG data output bit 1
MDOA0	I	TTL		Module A MPEG data output bit 0
MICLKB	O	TTL 3-state	Z	Module B MPEG clock input
MISTRTB	O	TTL 3-state	Z	Module B MPEG packet start input
MIVALB	O	TTL 3-state	Z	Module B MPEG valid data input
MDIB7	O	TTL 3-state	Z	Module B MPEG data input bit 7
MDIB6	O	TTL 3-state	Z	Module B MPEG data input bit 6
MDIB5	O	TTL 3-state	Z	Module B MPEG data input bit 5
MDIB4	O	TTL 3-state	Z	Module B MPEG data input bit 4
MDIB3	O	TTL 3-state	Z	Module B MPEG data input bit 3
MDIB2	O	TTL 3-state	Z	Module B MPEG data input bit 2
MDIB1	O	TTL 3-state	Z	Module B MPEG data input bit 1
MDIB0	O	TTL 3-state	Z	Module B MPEG data input bit 0
MOCLKB	I	TTL		Module B MPEG clock output to MPEG decoder
MOSTRTB	I	TTL		Module B MPEG packet start output
MOVALB	I	TTL		Module B MPEG valid data output

MDOB7	I	TTL		Module B MPEG data output bit 7
MDOB6	I	TTL		Module B MPEG data output bit 6
MDOB5	I	TTL		Module B MPEG data output bit 5
MDOB4	I	TTL		Module B MPEG data output bit 4
MDOB3	I	TTL		Module B MPEG data output bit 3
MDOB2	I	TTL		Module B MPEG data output bit 2
MDOB1	I	TTL		Module B MPEG data output bit 1
MDOB0	I	TTL		Module B MPEG data output bit 0

Modules command interface (24 pins)

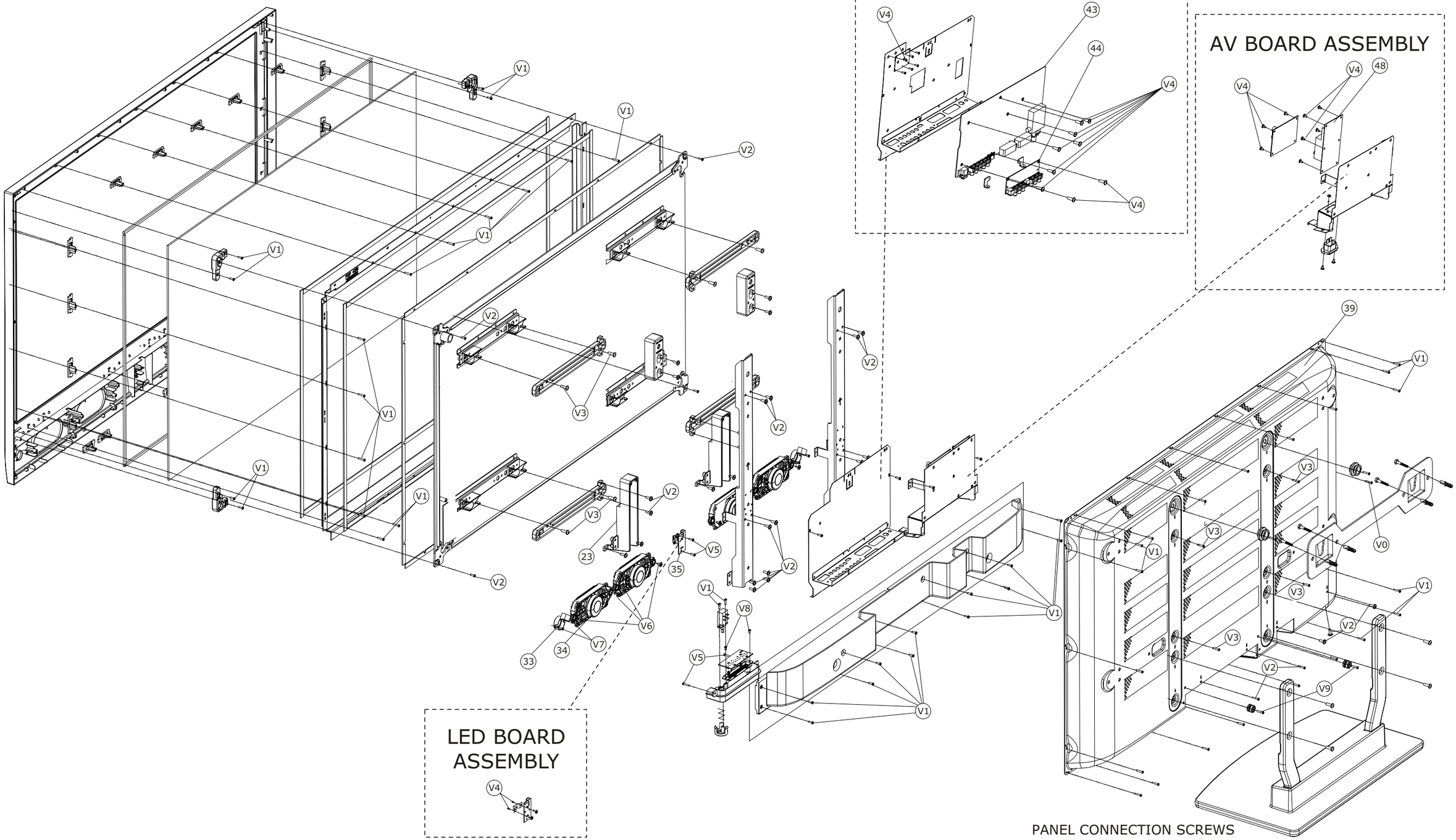
Name	I/O	Type	RST	function
RSTA	O	TTL 3-state	Z	Module A reset
CD1A#	I	TTL trig up		Module A card detect 1
CD2A#	I	TTL trig up		Module A card detect 2
CE1A#	O	TTL 3-state	Z	Module A card enable 1
CE2A#	O	TTL 3-state	Z	Module A card enable 2
RDY/IRQA#	I	TTL		Module A Ready / IRQ signal
WAITA#	I	TTL		Module A WAIT# signal
RSTB	O	TTL 3-state	Z	Module B reset (Internal scan out)
CD1B#	I	TTL trig up		Module B card detect 1
CD2B#	I	TTL trig up		Module B card detect 2
CE1B#	O	TTL 3-state	Z	Module B card enable 1
CE2B#	O	TTL 3-state	Z	Module B card enable 2
RDY/IRQB#	I	TTL		Module B Ready / IRQ signal
WAITB#	I	TTL		Module B WAIT# signal
REG#	O	TTL 3-state	Z	Modules REG# signal
OE#	O	TTL 3-state	Z	Modules output enable
WE#	O	TTL 3-state	Z	Modules write enable
IORD#	O	TTL 3-state	Z	Modules I/O read
IOWR#	O	TTL 3-state	Z	Modules I/O write
VCCEN	O	TTL 3-state	Z	Modules VCC switch control
DATOE#	O	TTL 3-state	1	External data buffers output enable
DATDIR	O	TTL 3-state	0	External data buffer direction
ADOE#	O	TTL 3-state	1	External address buffer output enable
ADLE	O	TTL 3-state	1	External address buffer latch enable

Power supply (9 pins)

Name	I/O	Type	Function
VCC_CORE		VDDI	Core Power
VCC_TSI		VDDE	I/O Power
VCC_TSO		VDDE	I/O Power
VCC_PROC		VDDE	I/O Power
GND_DVB2		VSSI	Core Ground
GND_CORE		VSSI	Core Ground
GND_TSI		VSSE	I/O Ground
GND_TSO		VSSE	I/O Ground
GND_PROC		VSSE	I/O Ground

18. APPENDIX A

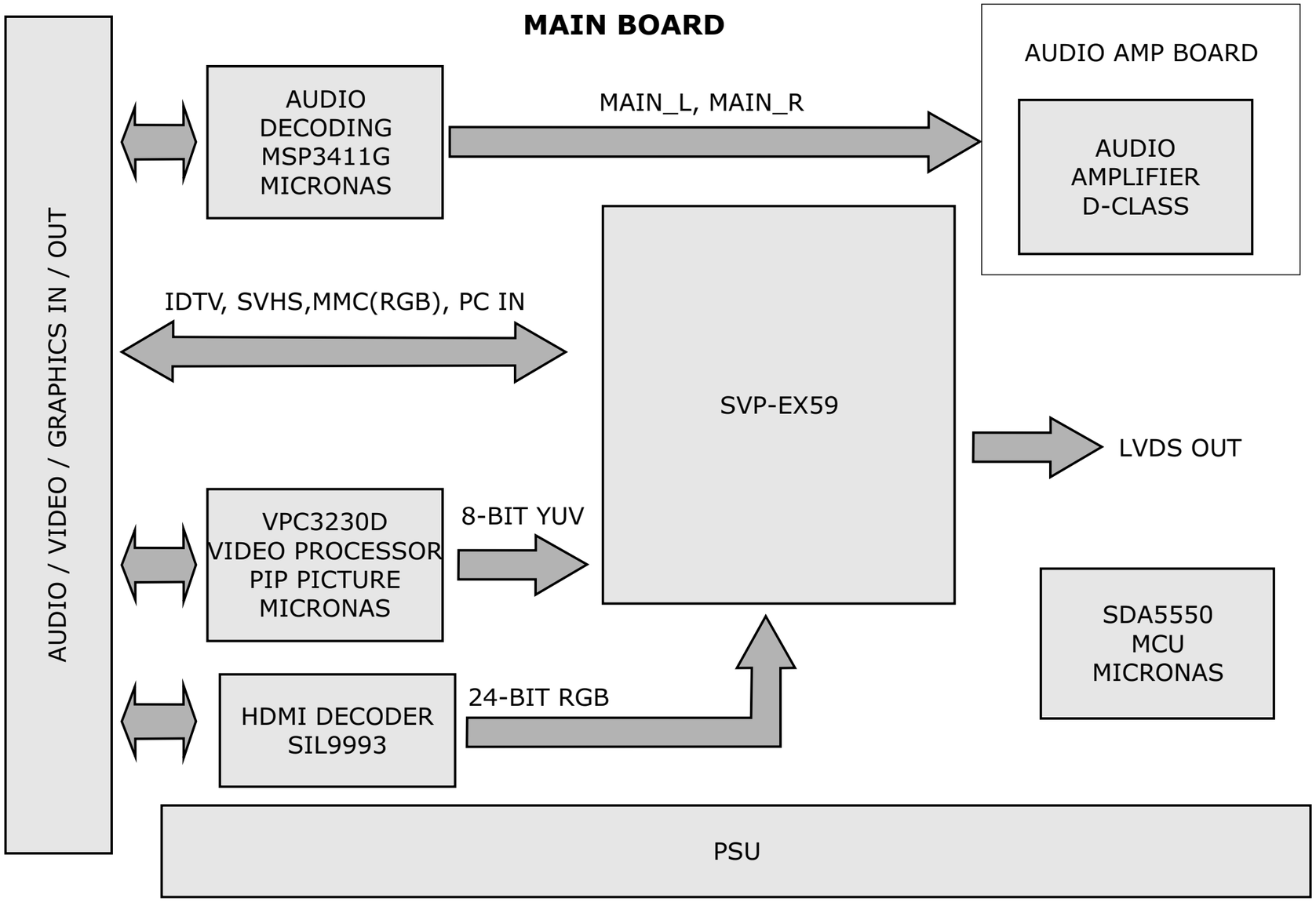
18.1. EXPLODED VIEW



SM012	ASSEMBLY DIAGRAM (EXPLODED VIEW)	HITACHI

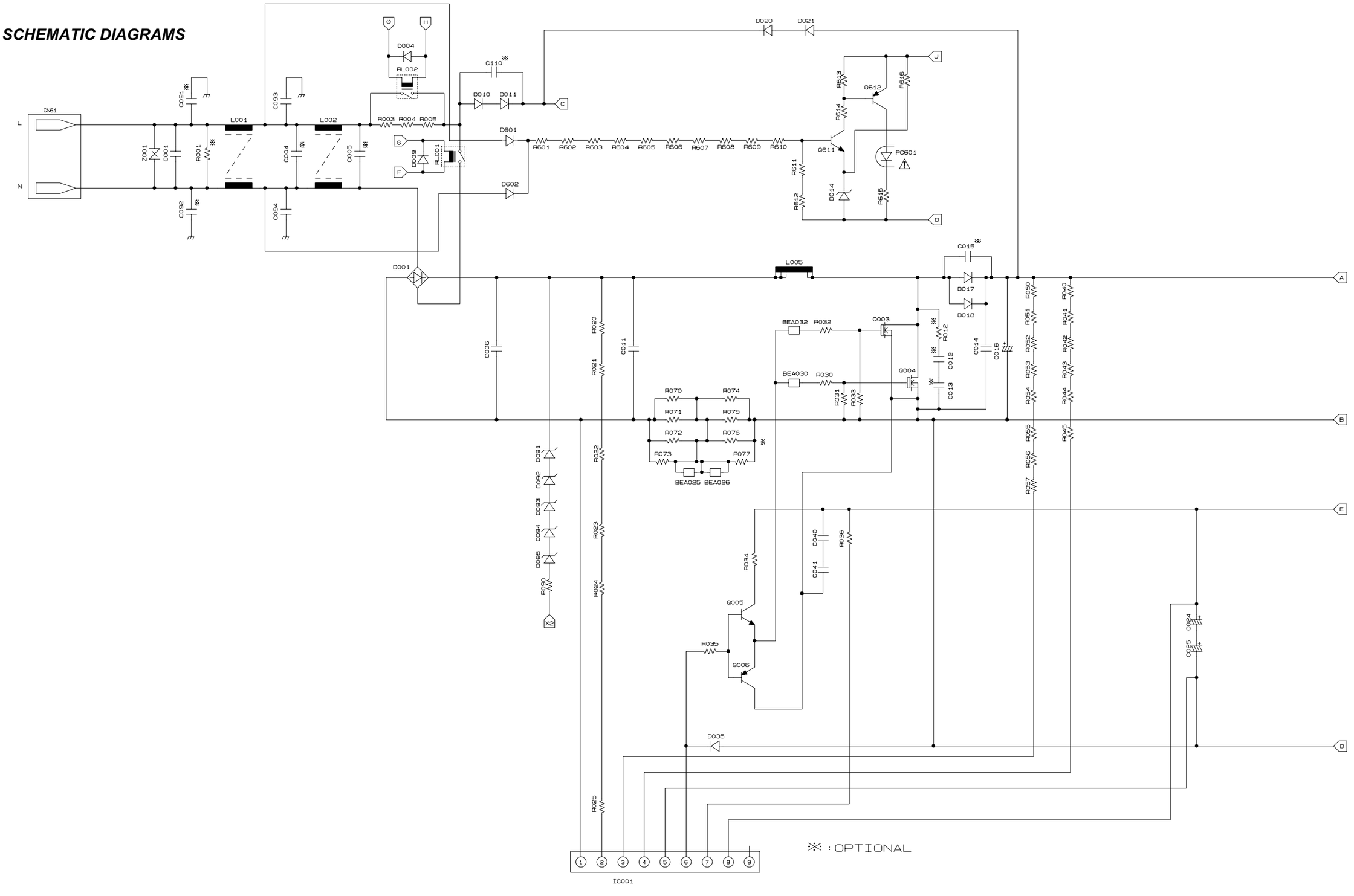
19. APPENDIX B

19.1. BLOCK DIAGRAM

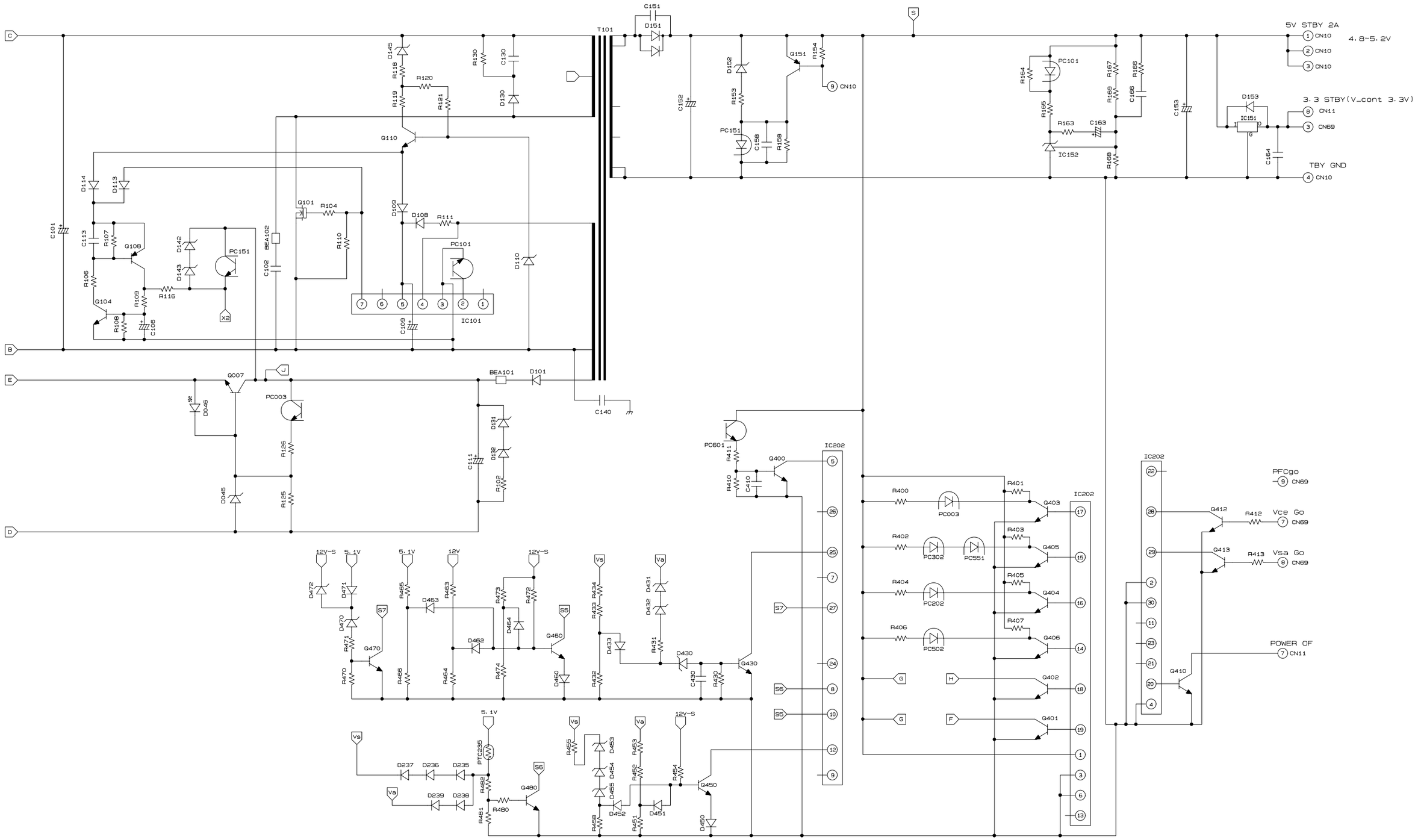


SM012	BLOCK DIAGRAM	HITACHI

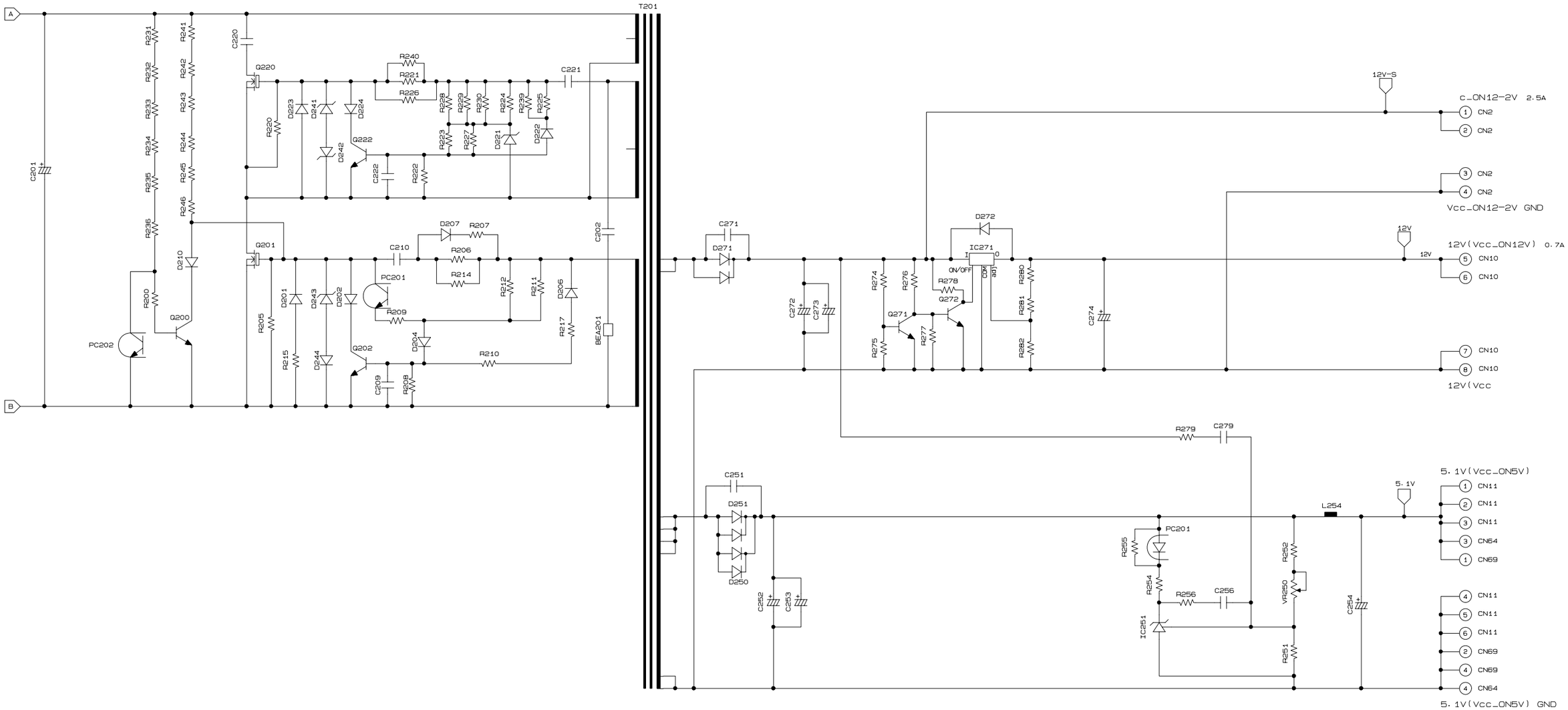
19.1. SCHEMATIC DIAGRAMS



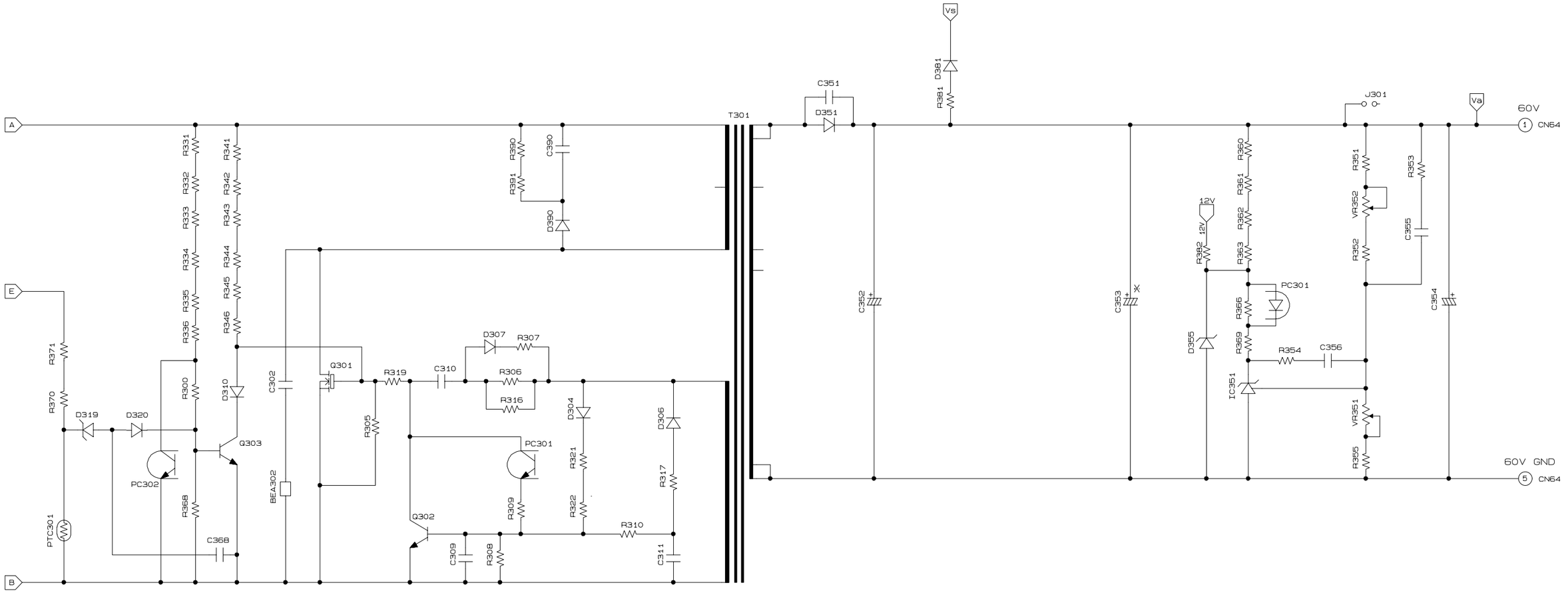
SM012	POWER BOARD - SHEET 1	HITACHI



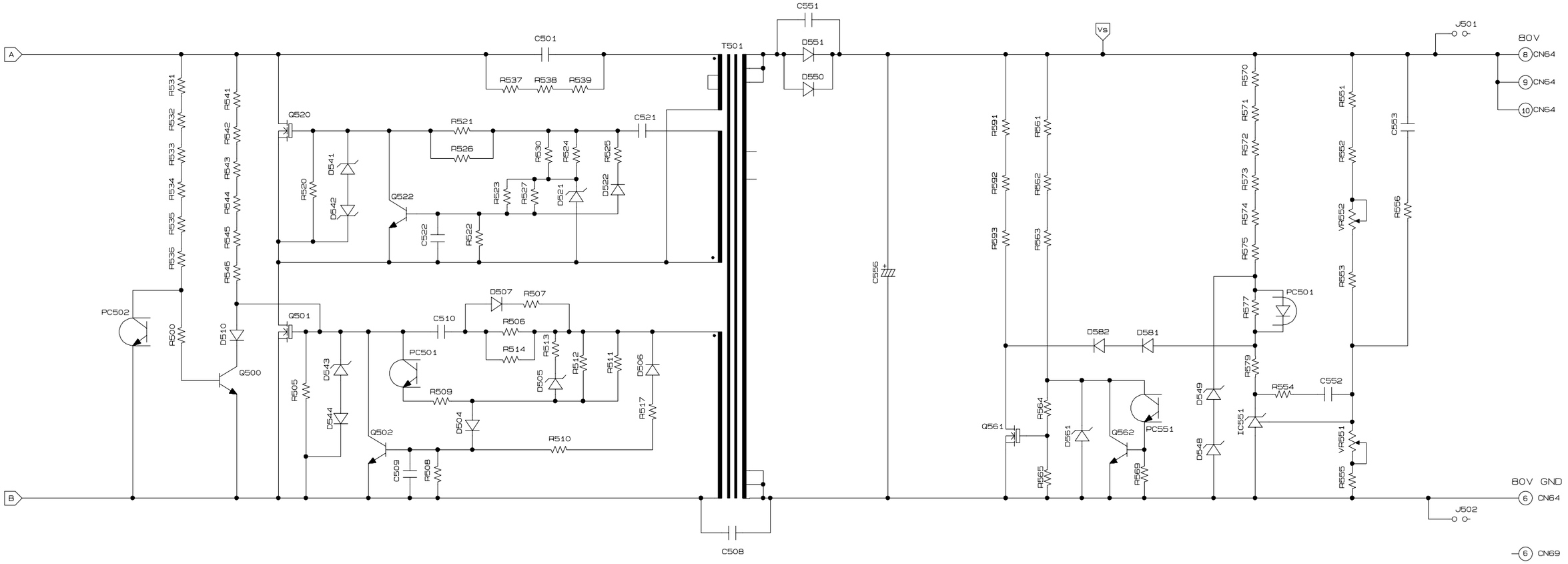
SM012	POWER BOARD - SHEET 2	HITACHI



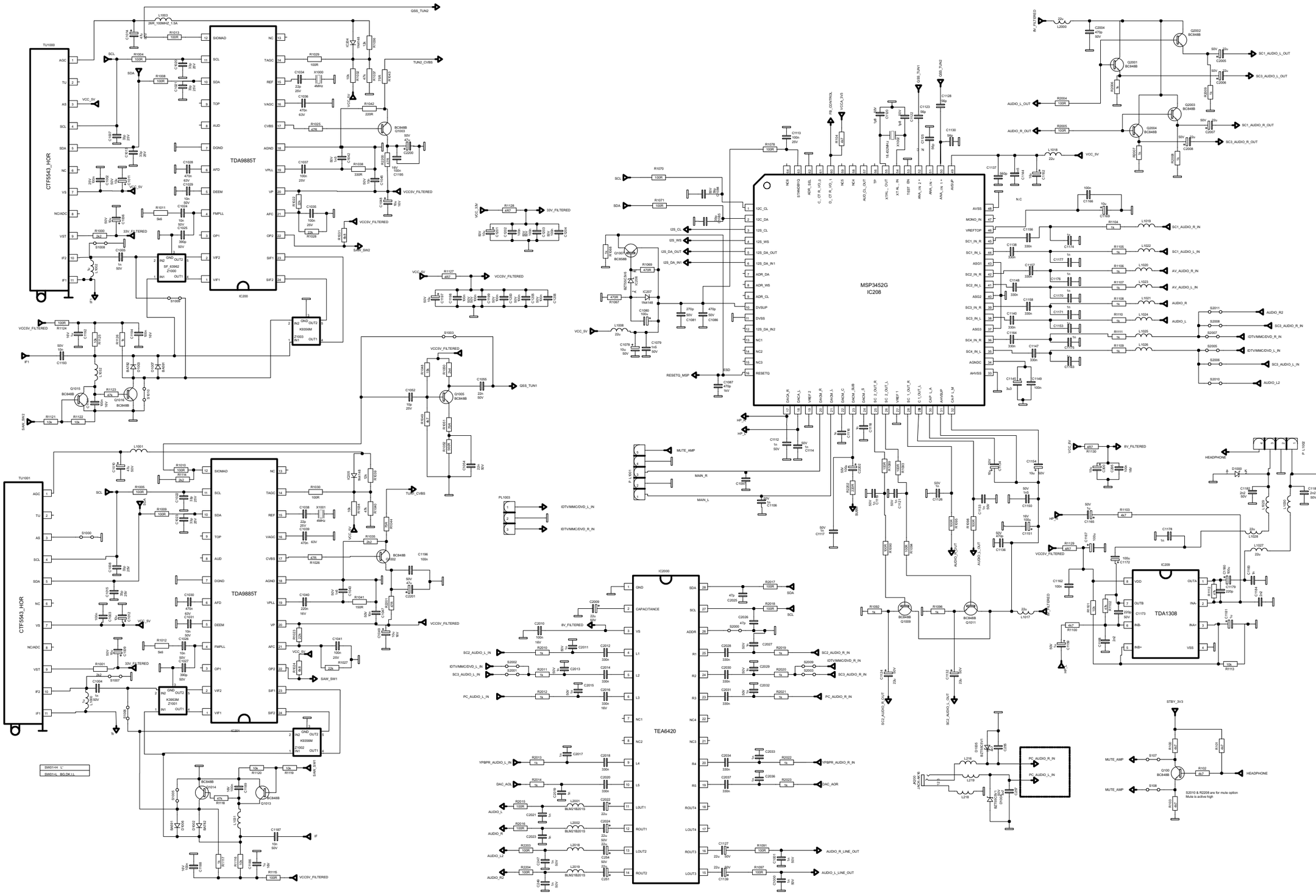
SM012	POWER BOARD - SHEET 3	HITACHI



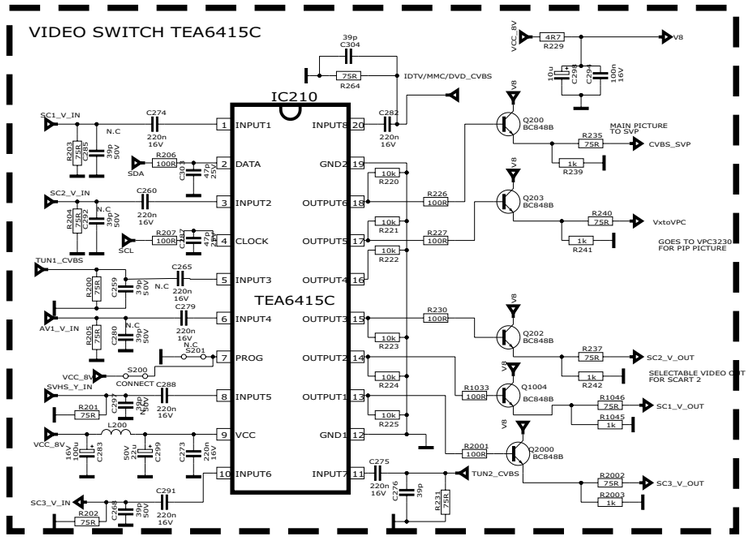
SM012	POWER BOARD - SHEET 4	HITACHI

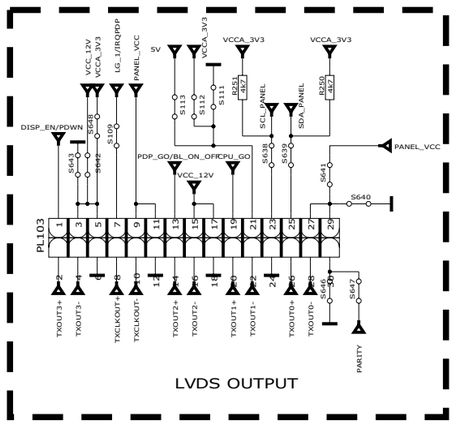


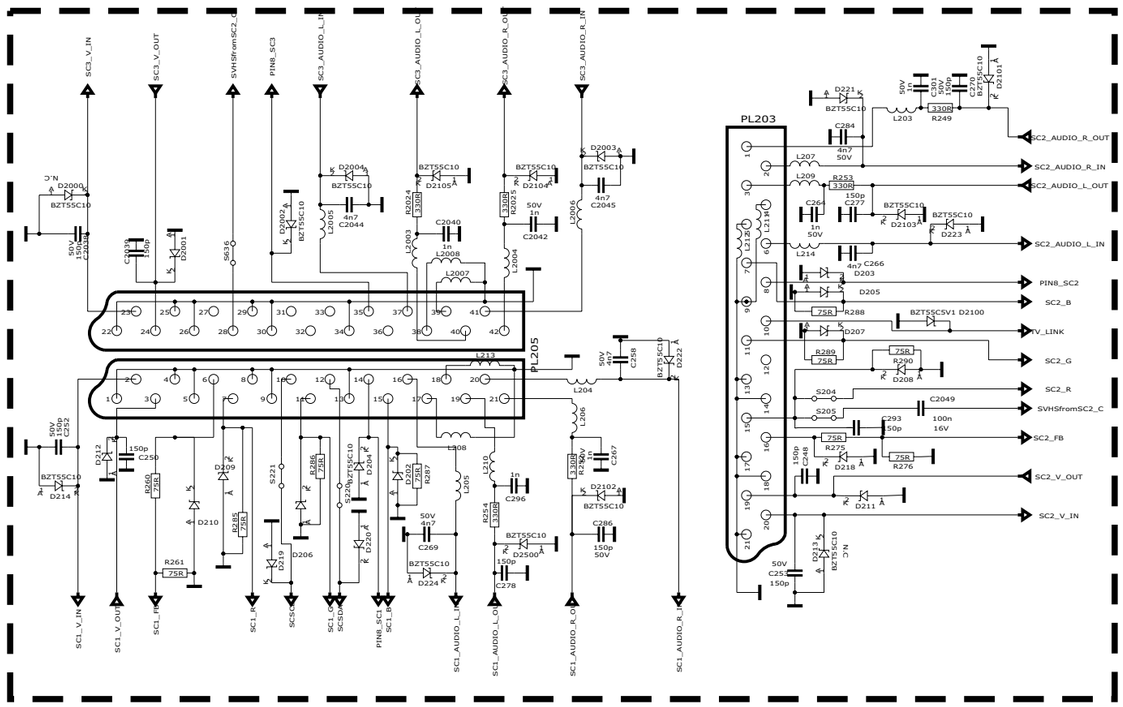
SM012	POWER BOARD - SHEET 5	HITACHI

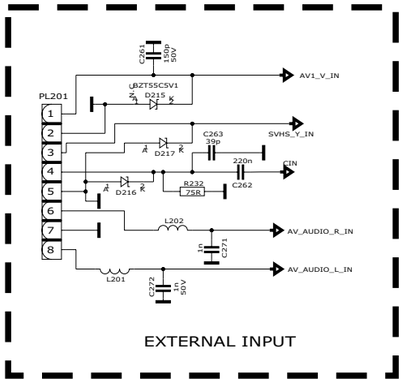


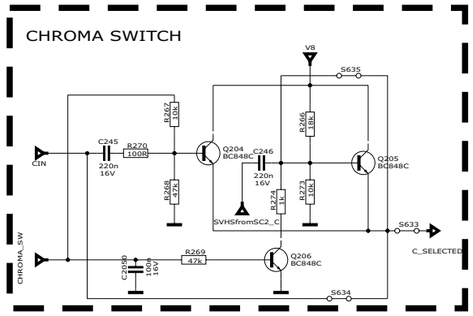
SM012	MAIN BOARD - TUNER/IF/AUDIO CIRCUIT	HITACHI

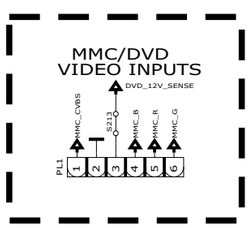


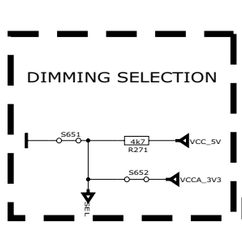


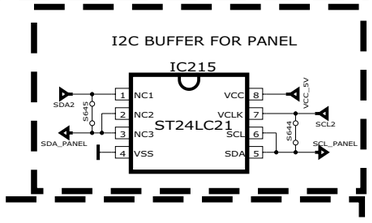


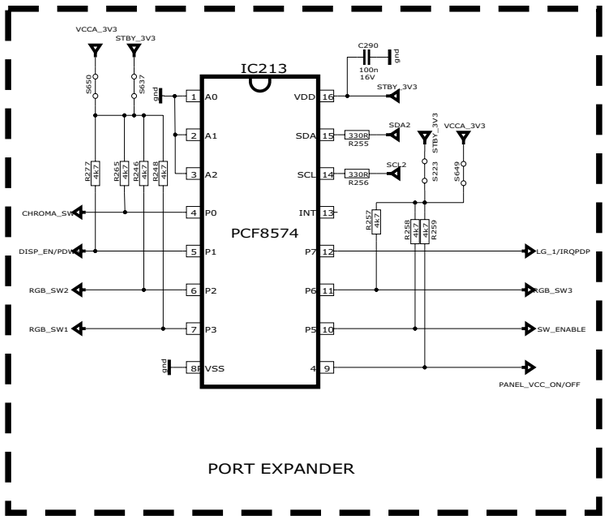


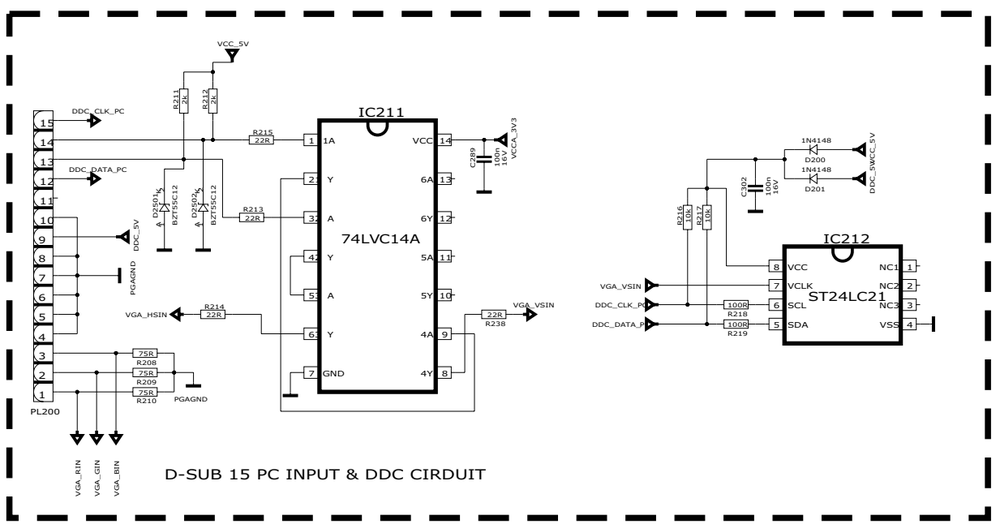


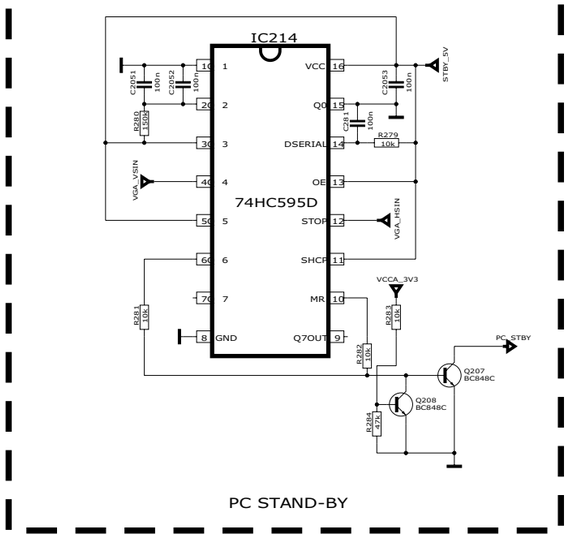




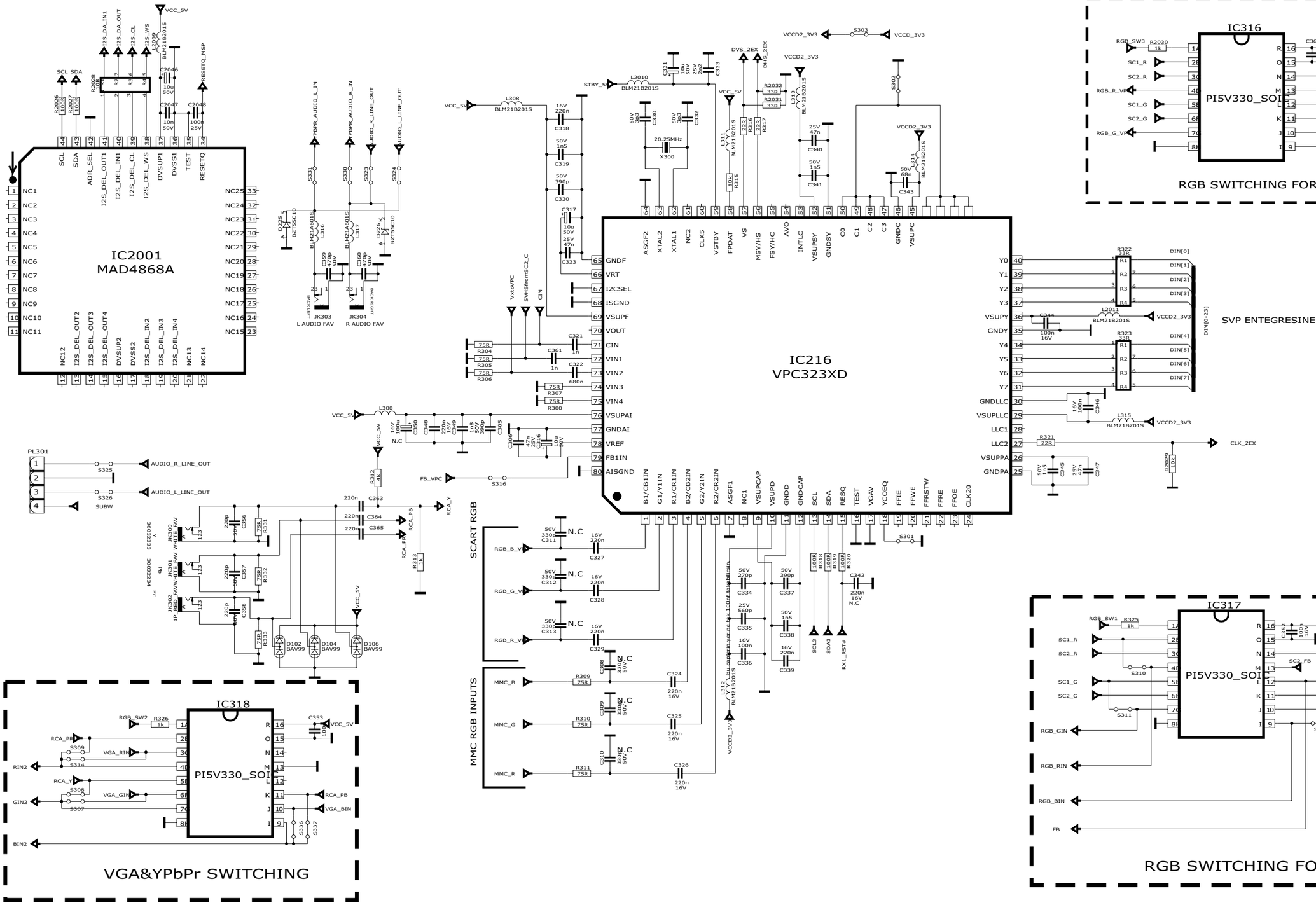








SM012	MAIN BOARD - IN/OUT CIRCUITS	HITACHI



SM012	MAIN BOARD - VPC3230 CIRCUIT	HITACHI

DIGITAL IDTV INPUTS [ITU 601]

PC&YPbPr INPUT

MAIN PICTURE

MAIN RGB INPUT

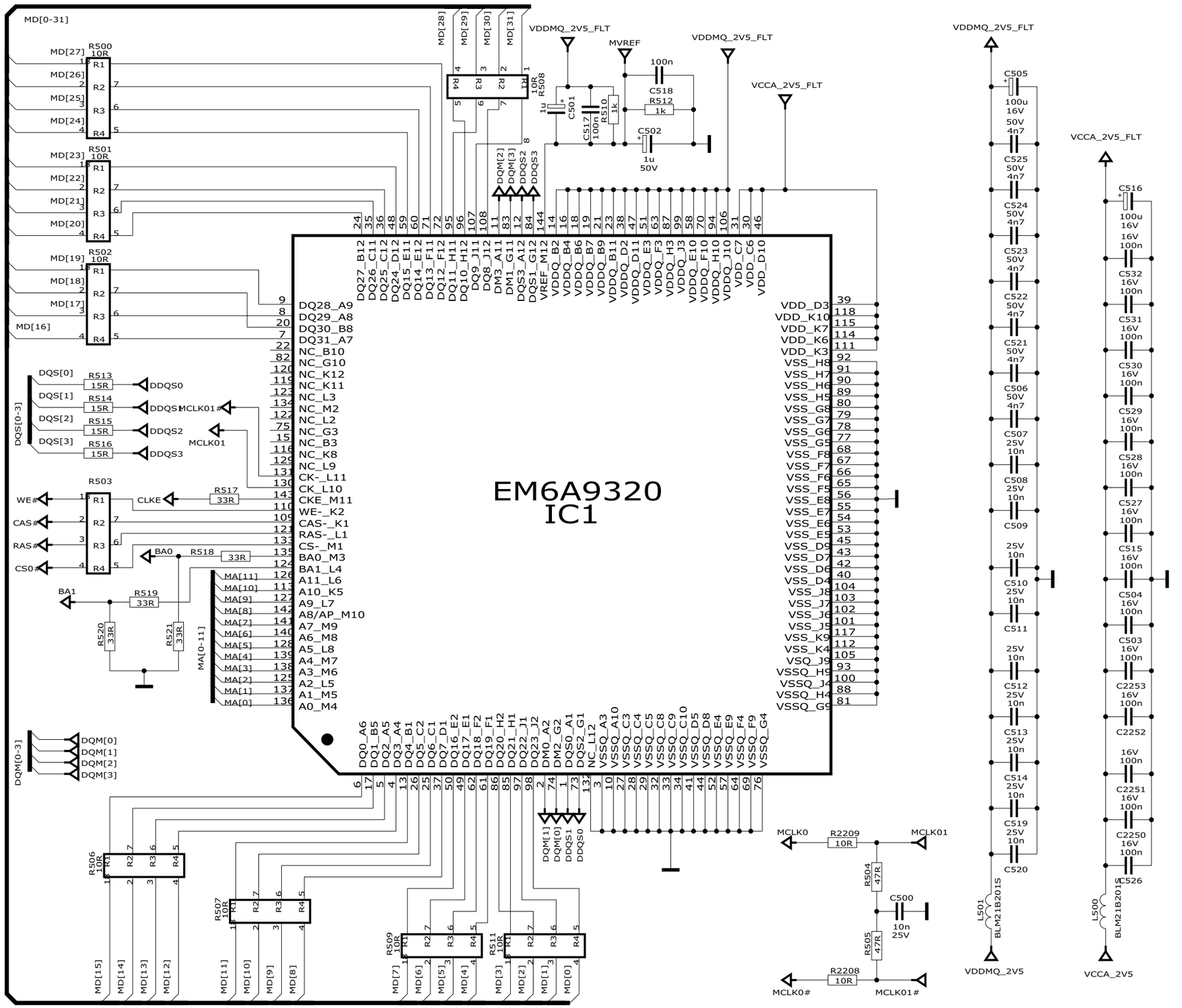
IC224
SVP_EX_51

LVDS OUT

DIGITAL SIN

IC107
74LX1G86STR

SM012	MAIN BOARD - VIDEO DECODER CIRCUIT	HITACHI



SM012	MAIN BOARD - DDR RAM CIRCUIT	HITACHI

IC217 K6R4008V1C-I/C-P

IC219 M29W040B
CORRESPONDS TO Winbound W27E040 EPROM & ST M29F040 Flash

IC220 SDA5550M

IC622 GAL16LV8

IC218 24LC32A

BRIGHTNESS CONTROL

CIRCUIT OF SW UPDATE FROM SCART2

LEVEL SHIFTER

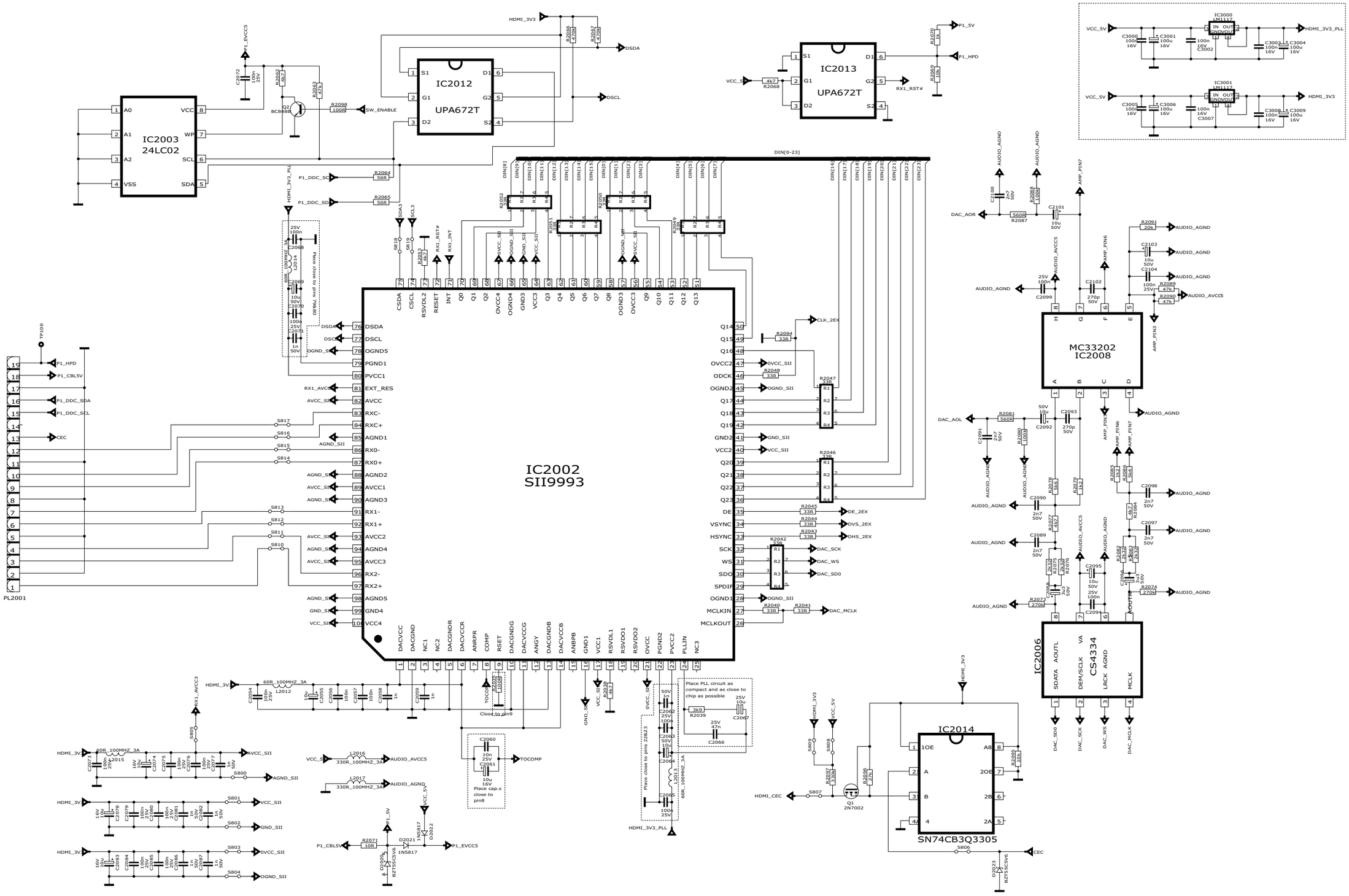
E2

UART SOCKET FOR IDTV

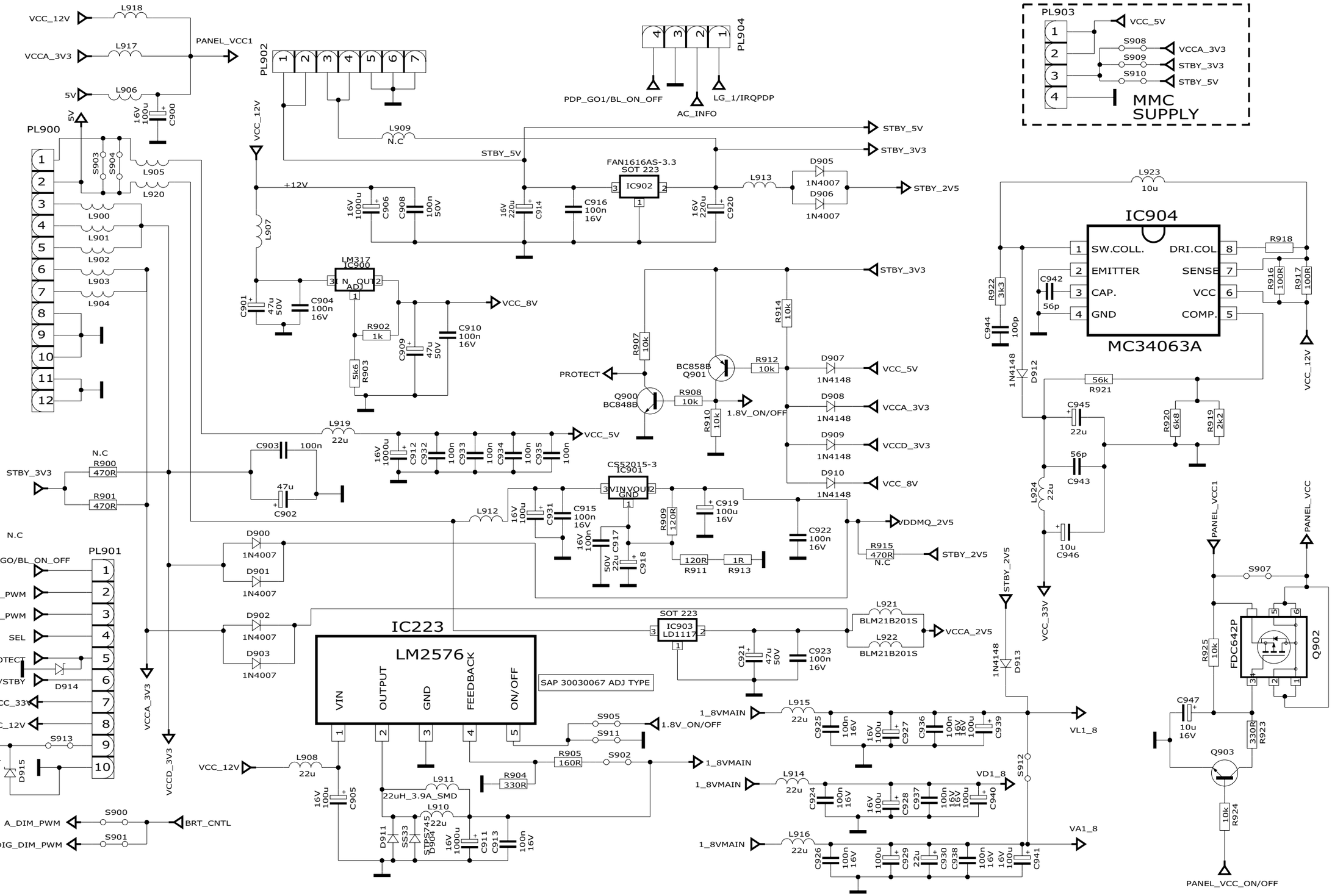
MMC_IR GIRISI

TV-LINK

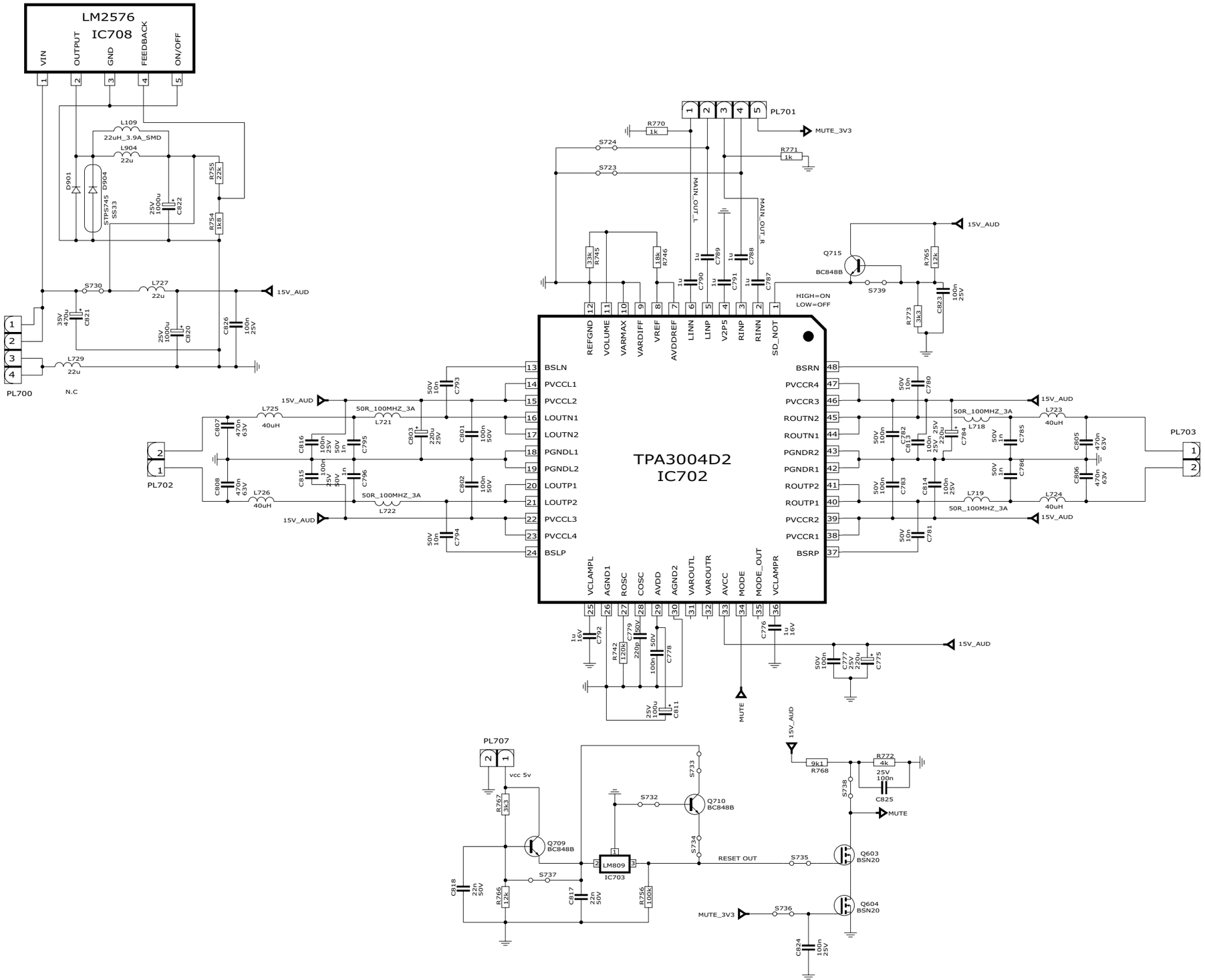
SM012	MAIN BOARD - MCU INTERFACE CIRCUIT	HITACHI



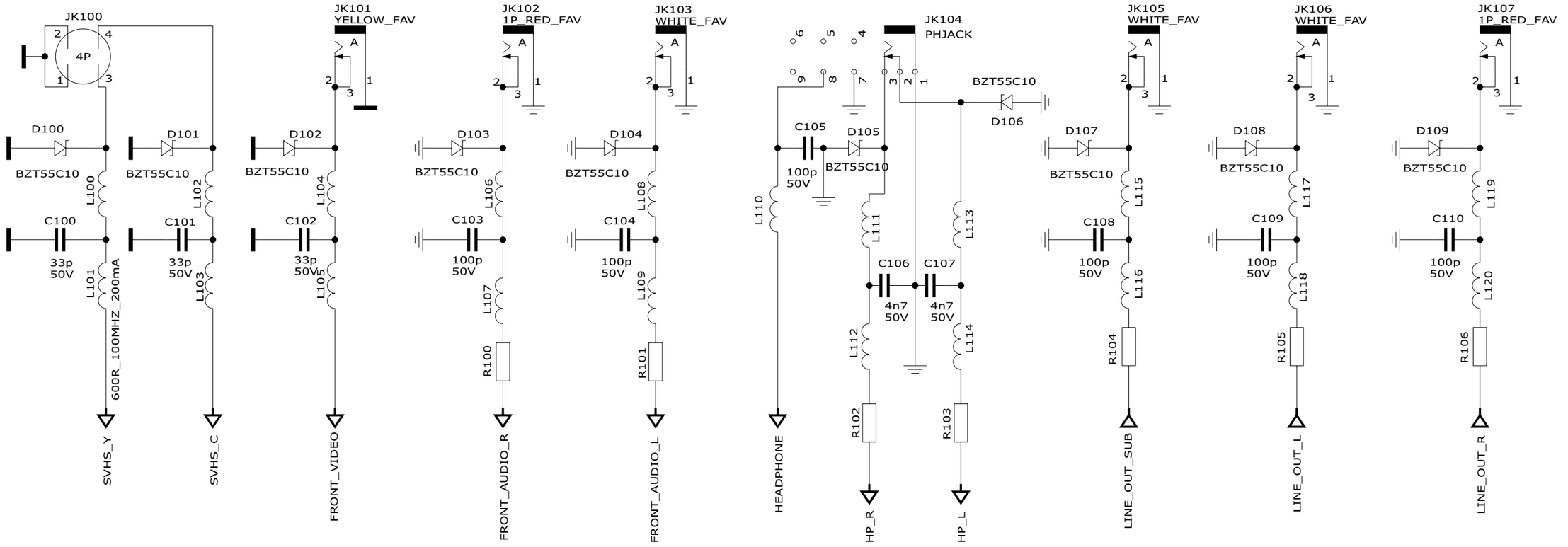
SM012	MAIN BOARD - HDMI/DAC CIRCUIT	HITACHI



SM012	MAIN BOARD - POWER SUPPLY CIRCUIT	HITACHI



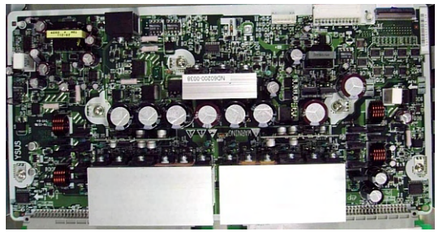
SM012	AMPLIFIER BOARD - D-CLASS AMPLIFIER CIRCUIT	HITACHI



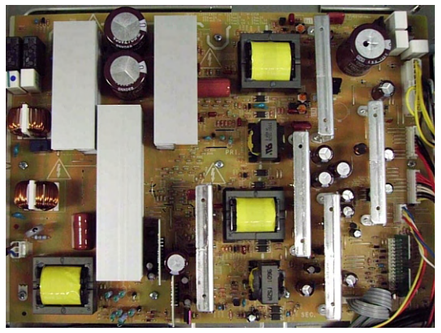
SM012	FRONT AV BOARD CIRCUIT	HITACHI

19.3. CIRCUIT BOARDS

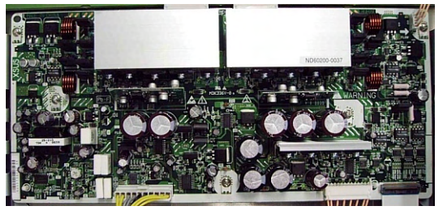
1. Y-SUS Board (TS06288)

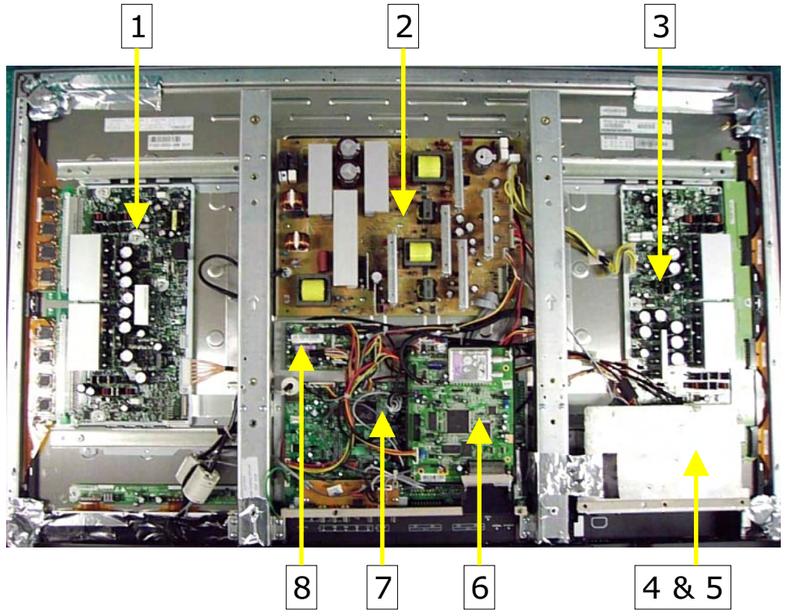


2. Power Board (VS30043468)

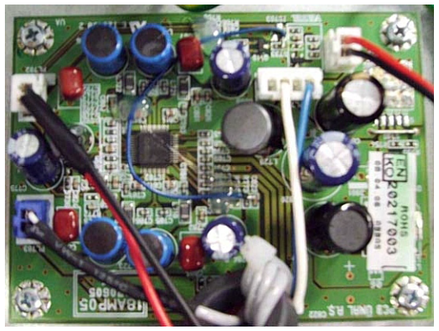


3. X-SUS Board (TS06287)

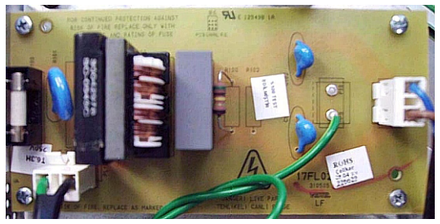




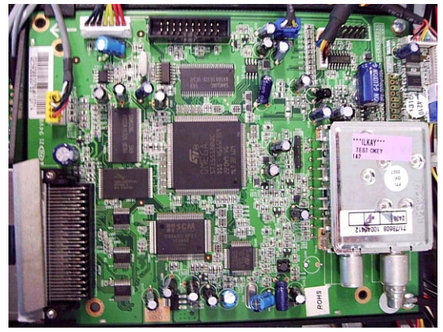
4. Audio Board 18AMP05 (VS20217003)



5. Filter Board 17FL2-02 (VS20225622)

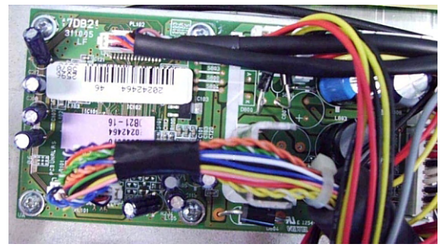


6. IDTV Board 17DB23 (VS20252456)

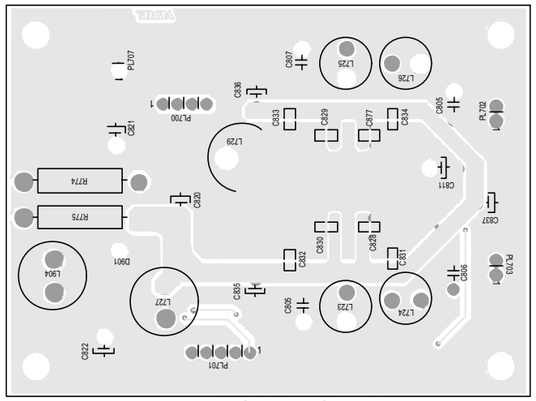


7. Main Board 17MB15-E5 (VS20251818)

8. Joint Board 17DB21 (VS20252456)

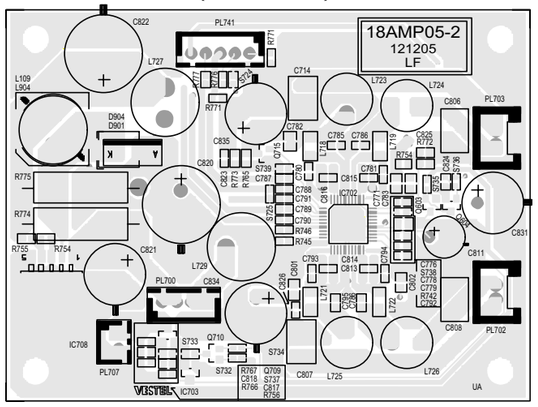


19.4 PCB LAYOUTS

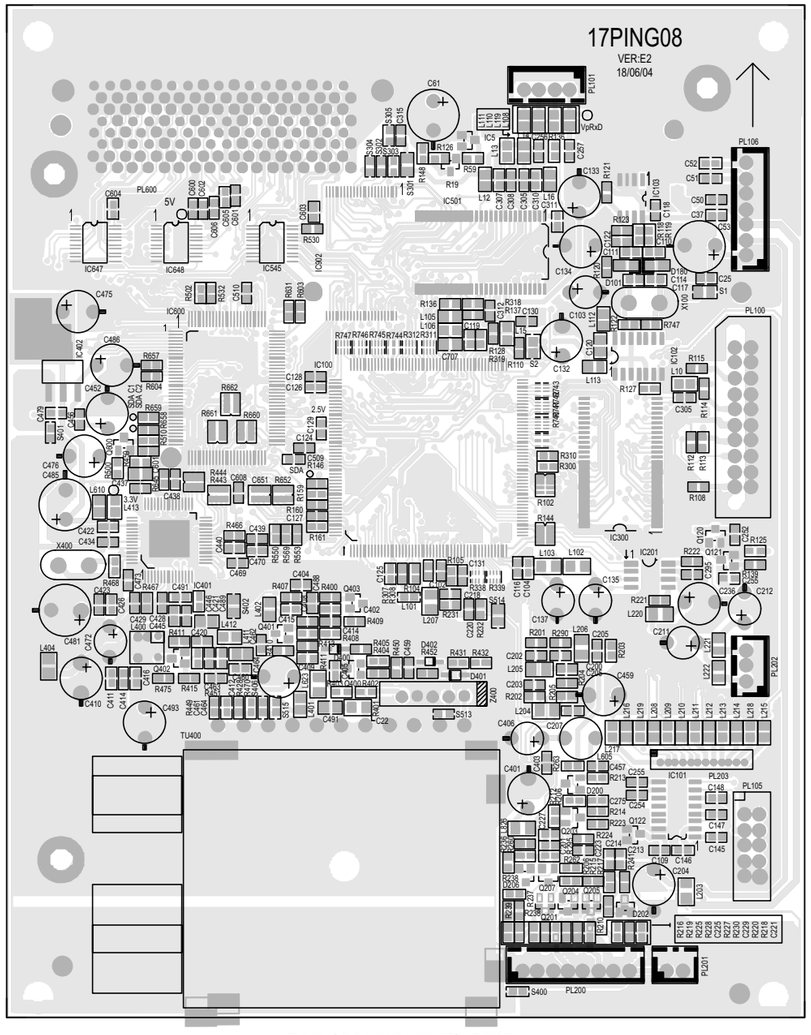


BOTTOM (SOLDER) SIDE

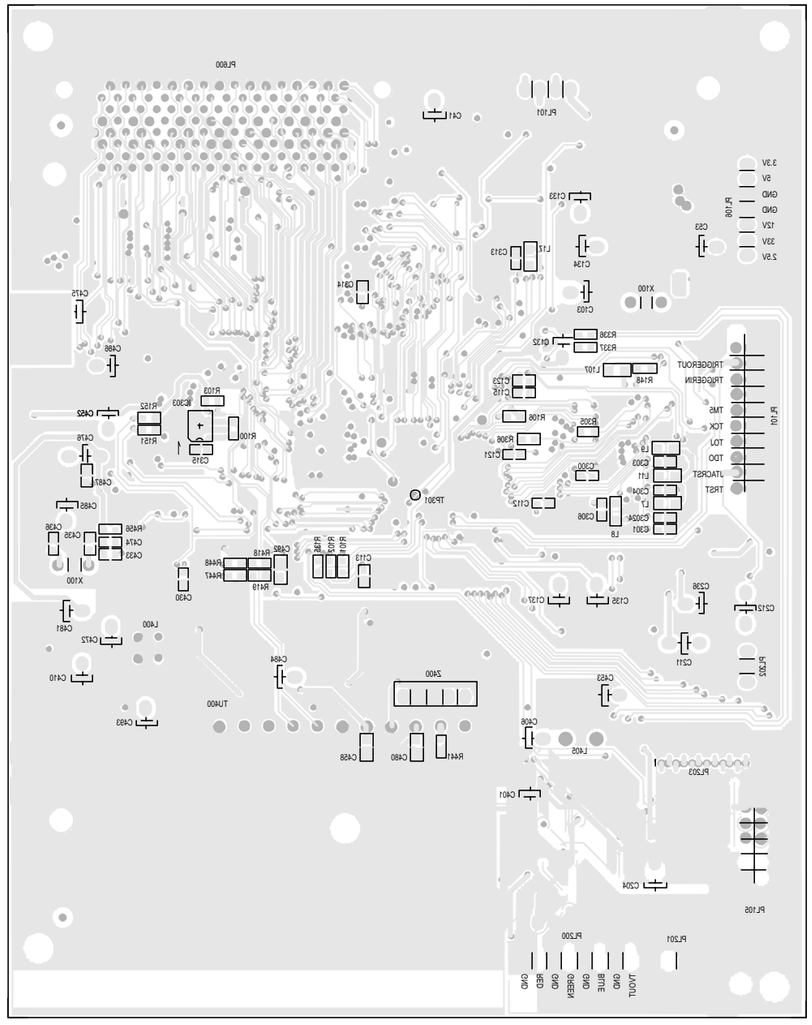
TOP (COMPONENT) SIDE



AMPLIFIER BOARD

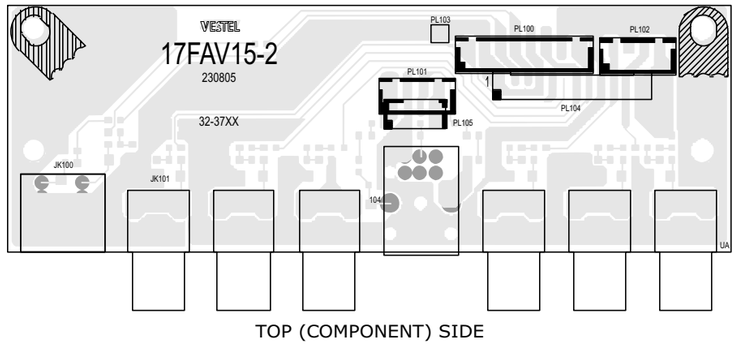


TOP (COMPONENT) SIDE

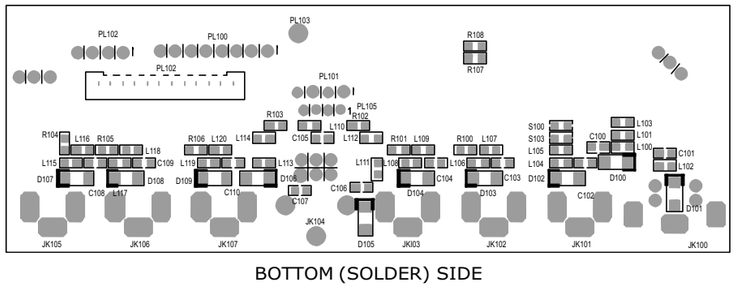


BOTTOM (SOLDER) SIDE

IDTV BOARD



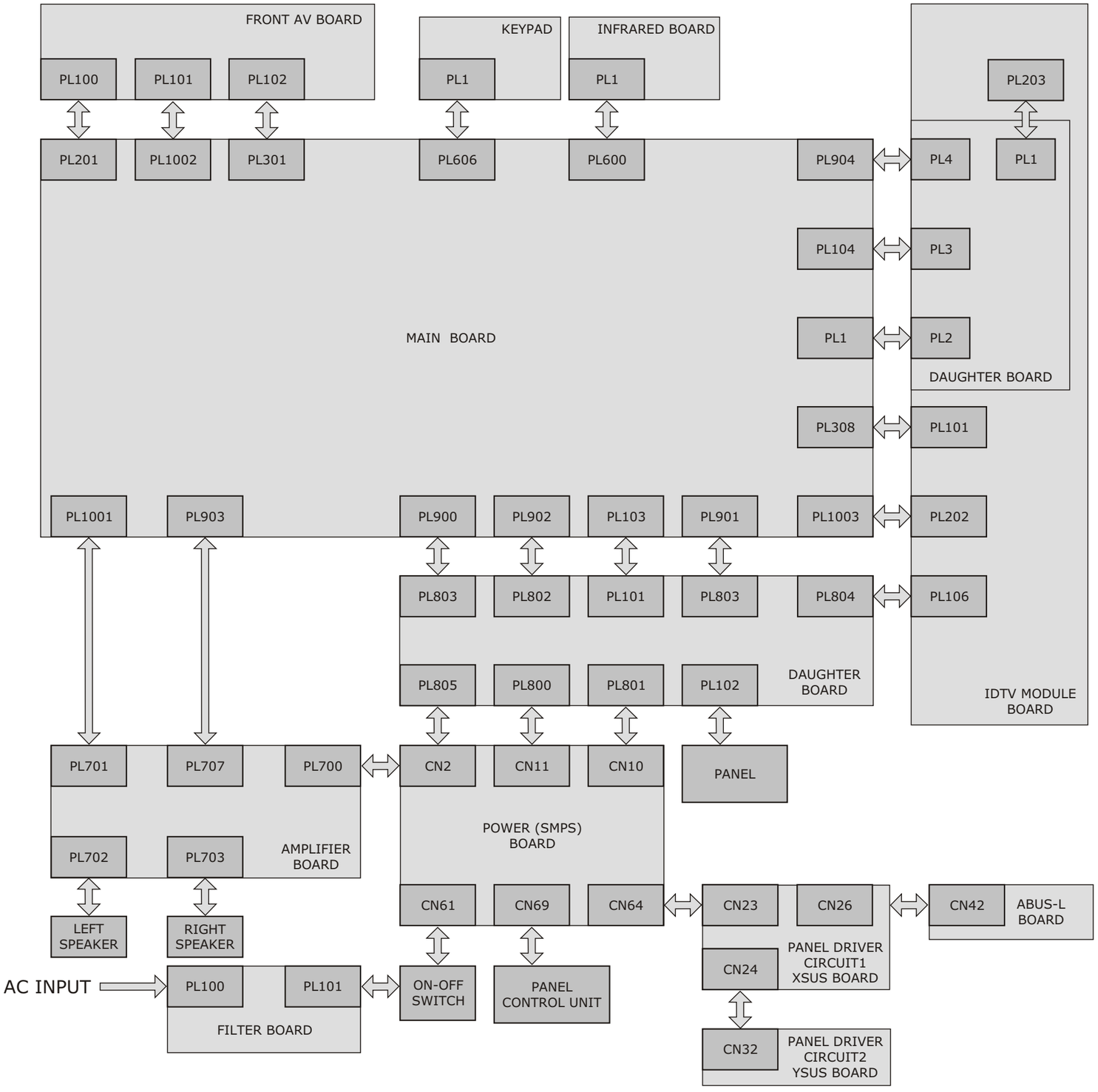
TOP (COMPONENT) SIDE



BOTTOM (SOLDER) SIDE

FRONT AV BOARD

19.4. CONNECTOR DIAGRAM



THE UPDATED PARTS LIST

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